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MEASUREMENT AND FIELD SIMULATION BASED CHARACTERIZATION OF PLASTIC IC PACKAGES

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ABSTRACT

A method to obtain electrical models for IC packages is introduced. We used measured S-parameters to extract equivalent circuits for the package and surrounding components. The resulted equivalent circuit was verified with 3D field simulation.

DEVICE UNDER TEST (DUT)

One of the main problems at package characterizations is that the internal ends of the lead-frame pins are not accessible without significant modification on the investigated structure as was reported in [1]. To overcome the need for this modification we put a special test-chip into the package with well characterized termination on it. This test-chip provided open/load/short termination for the bondwires connecting the lead-frames with the bond-pads on the chips. This way the whole structure under investigation consisted of the test-chip, the bondwires, the lead-frame and the printed circuit board (PCB), which held the package and provided the connections for the measurement equipment. The PCB was prepared to make the selection of any two pins possible to form the two-port to be measured.

MEASUREMENTS

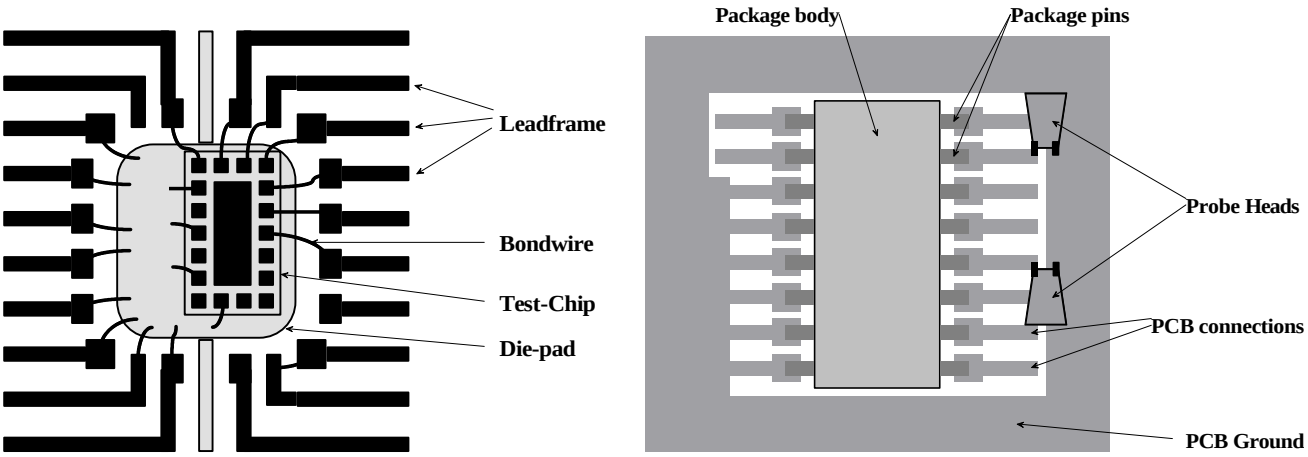
At a given test package (package with test-chip inside) we carried out several 2-port S-parameter measurements by a standard vector network analyzer (VNA) up to 6 GHz. To connect the DUT to the VNA a Cascade Probe-Station was used with ACP40 probe-heads with 0.5 mm pitch size. This allowed us to use one single package for the whole set of measurements by simply moving the probe-heads from pin to pin, while all the unmeasured pins remained untouched. The selection of pin-pairs contained the pins beside each other, pins having one untouched in between, fixing one pin at the corner and moving the other around.

Since the packages are symmetrical structures we measured only at one side of the packages while the other side was used to provide ground connections for the die-pad inside the package by multiple down-bonds from that leads to the die-pad. There were some leads connected directly by bondwires together to make the separation of the bondwire and lead-frame related inductance possible. The measured data (2-port S-parameters) were transferred into a CAD environment to use them at the parameter extraction. See Figure 1. for the whole setup.

PARAMETER EXTRACTION

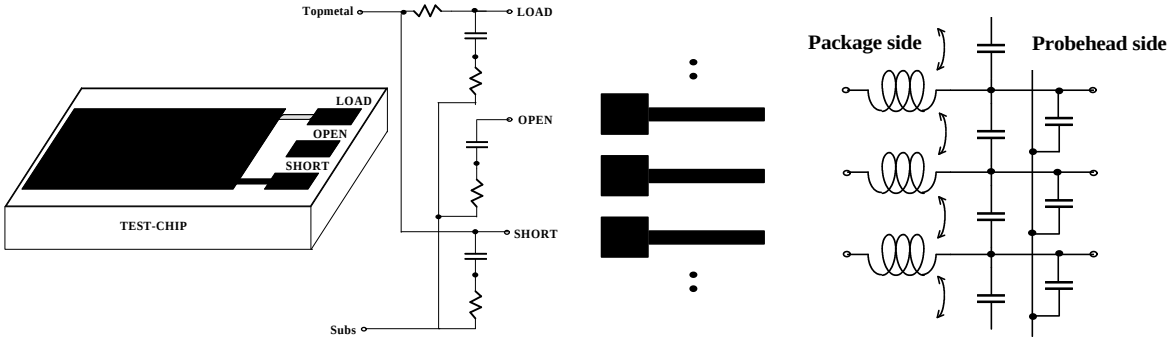
As a first step equivalent circuits were defined for all components the DUT consists of. We measured the open/load/short termination by on-wafer measurements on the test-chips before the wafer was cut. The parallel (multicoupled) PCB lines were characterized by measurements too. The equivalent circuits for these parts were defined first, where the parameters of the equivalent circuits were obtained by making the measured and simulated parameters equal. For

this step an optimization was defined with commercial CAD tool (HP-MDS), where the goal to be minimized was the difference between the measured and simulated S-parameters and the circuit parameters were the variables. The optimization resulted in the equivalent circuit for the test-chip loads and for the PCB lines which are shown on Figure 2.a and Figure 2.b



a. DUT setup (inlet, lead-frame, bonding) b. PCB layout with probe head connection

Figure 1



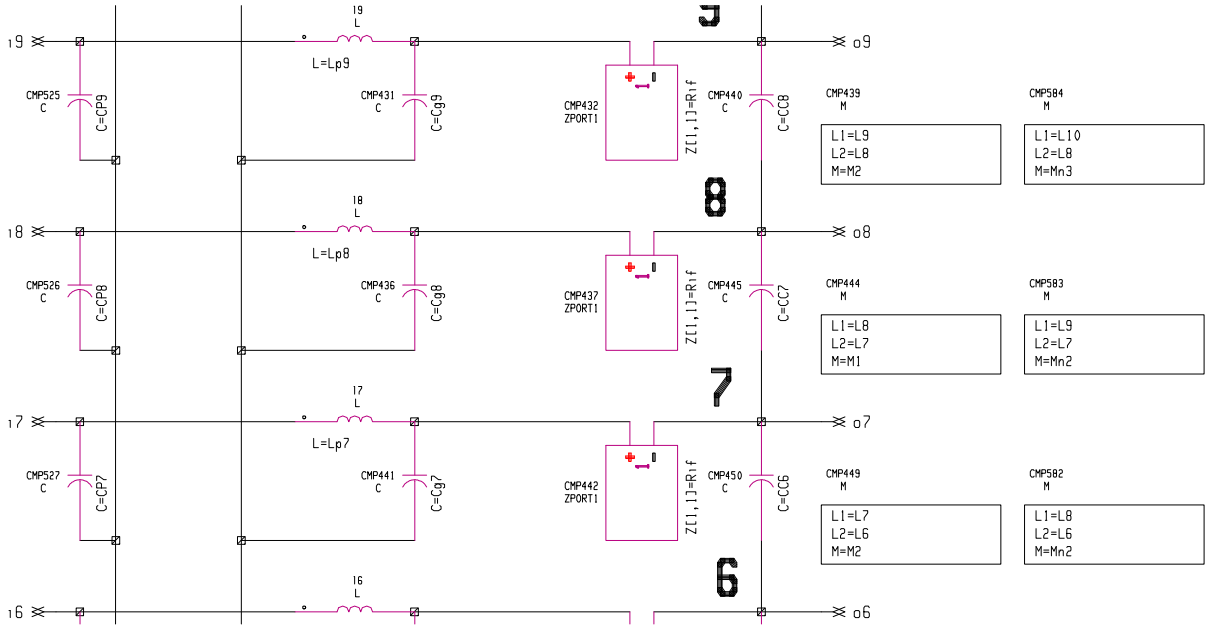
a. The equivalent circuit for the test-chip loads b. The equivalent circuit PCB lines

Figure 2

As a next step the equivalent circuit for the bondwires and for the lead-frame had to be defined. For the bondwires serial inductors with coupling to the neighbors and the next non adjacent wires were defined. For the lead-frame pins serial and mutual inductance, coupling capacitance, ground capacitance to the PCB ground and coupling capacitance to the die-pad was defined (see the representative parts of the schematic on Figure 3.) according the well known schematics used before [1,2,3]. We included mutual coupling not only at the neighboring pins but between the further ones too (i.e. between 1-3, 2-4, 3-5 ... etc. pins). At the internal ends of the leads we added capacitance to the paddle too. The die-pad was split into tree parts in the equivalent circuit. The dummy leads between the corner pins were represented by an inductor with coupling to the neighbors as the normal pins. This additional part provided a much better description for the corner area, and made the reason of the coupling between pins in the opposite corners visible.

Having the schematics defined the same optimization procedure was defined as at the test-chip and PCB line characterization. Here the test-chip and the PCB lines were taken into account

with their previously fixed equivalent circuit parameters. The bondwires and the lead-frame had undefined equivalent circuit parameters. For the parameter extraction (finding the undefined circuit parameters) several measurement positions were taken into account simultaneously. We selected pin positions from the corner area, from the middle one and from area where the internal lead-ends were connected directly. We utilized the symmetry to reduce the number of variables for the optimization at all possible places.

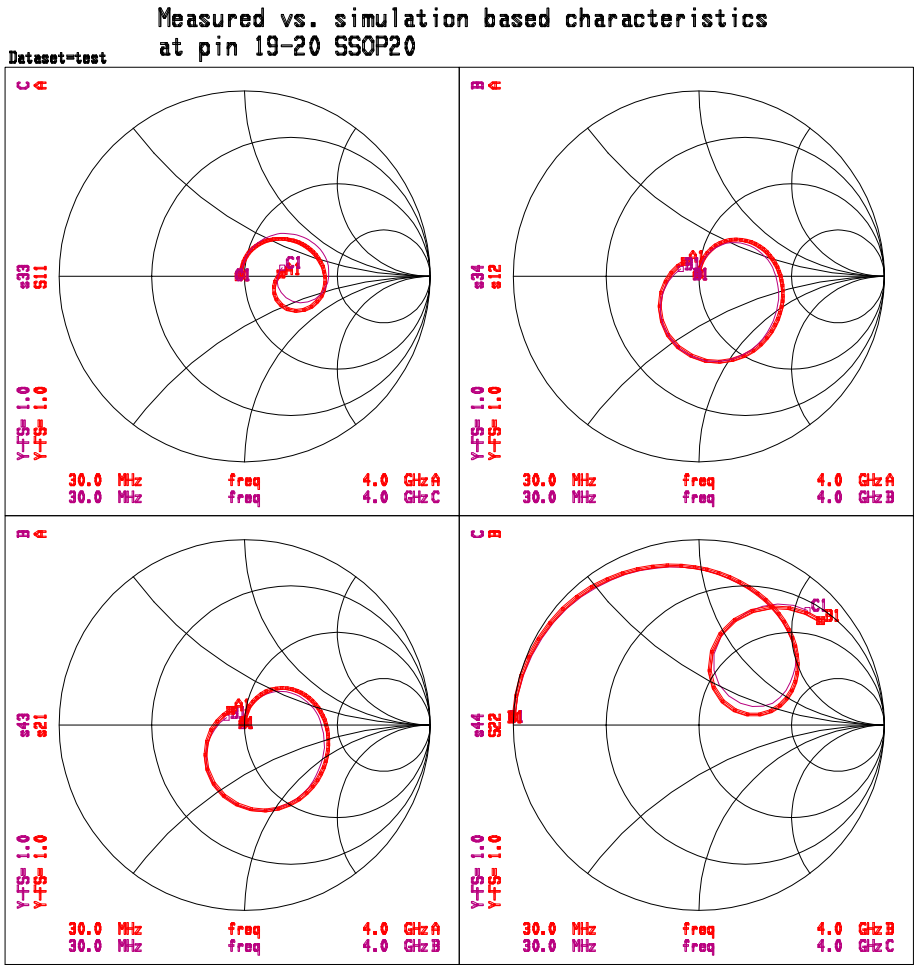


Equivalent circuit of the middle part of a leadframe
Figure 3

If the agreement between measured and simulated parameters could not be improved after a few optimization steps the equivalent circuit had to be modified according the observed differences. At the end we got very good agreement between the measured and simulated parameters as it is shown on Figure 4.

3D FIELD SIMULATION

We compared the results of our measurement based package characterizations with the results of a commercial 3D filed simulator (Ansoft Quick 3D Parameter Extractor [4]). This tool solves the reduced Maxwell equations taking only the static fields into account, so its validity is limited by the overall geometry/wavelength ratio. As long as the overall lead lengths are smaller than a fraction of the wavelength, this field simulation gives correct results and in the same way lumped equivalent circuits can be used for modeling the behavior of the packages. At SOIC packages this gives an upper limit around 2.5GHz. Changing the measurement based lead-frame model to the field simulation based one we compared the measured parameters again with the new 3D filed simulation based ones. The agreement was as good as before indicating that both methods (measurement and filed simulation based) can correctly describe the electrical performance of the package.



Measured and simulated S-parameters at pins 19-20 at an SSOP20 package
Figure 4.

CONCLUSION

The described methods proved to be able to extract equivalent circuit parameters for IC packages used in the RF wireless applications. This makes it possible for Austria Mikro Systeme to supply its customers with correct, measurement verified package models. This way designers can take all parasitic effects caused by packaging into account in the early circuit design phase already.

REFERENCES

[1] Chi-Taou Tsai, Wai-Yeung Yip: "An experimental Technique for Full Package Inductance Matrix Characterization," *IEEE Trans. Comp., Packag., Manufact. Techn. part B*, vol.19, No.2, pp 338-434, 1996

[2] Robert W. Jackson: "A Circuit Topology for Microwave Modeling of Plastic Surface Mount Packages," *IEEE Trans. on Microwave Theory and Techniquies*, vol.44. No.7. pp1140-1146, 1996

[3] Brian Young, Aubrey K. Sparkman: "Measurement of Package Inductance and Capacitance Matrices," *IEEE Trans. Comp., Packag., Manufact. Techn. part B*, vol.19, No.1, pp 225-229, 1996

[4] *Maxwell Quick 3D Parameter Extractor*, Ansoft Corp, 1994