RF CMOS Models - Enablers for Portable Communication SoCs

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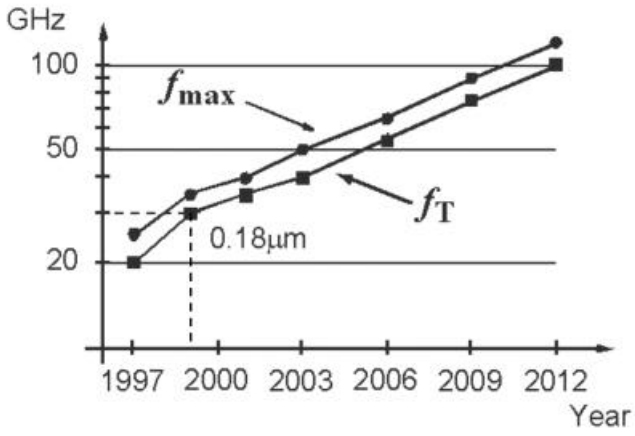
These are exciting times for the communications industry. Technological advances and the ever-escalating demand for pervasive access to information have converged to signal the arrival of a new era of personal and portable communication devices. Applications and products centered on 3G, WAP (Wireless Application Protocol), HomeRF and Bluetooth are on the verge of proliferating in the marketplace. In order to make these devices attractive to the consumer, a technology that can satisfy both high-speed design constraints and provide low cost must be available.

Current CMOS technology is a viable candidate. As Figure 1 shows, modern deep-submicron MOS transistors have more than enough speed to handle high-frequency or RF signals. For example, applications such as wireless LAN (as set forth by IEEE Standards 806.11b and 806.11a) operate at 5 GHz; such applications can be implemented entirely in CMOS technology. This will allow for maximum integration of the RF front end, baseband logic, custom analog and memory modules for a system on a chip (SoCs). Integration also allows systems makers to drive down manufacturing costs.

Figure 1. The current generation of CMOS has more than enough speed to handle today's wireless communications devices. Source: SIA Technology Roadmap



While the semiconductor performance capability is readily available, EDA design tools have yet to fully learn and embrace the intricate physical phenomena at high speeds of operation. Without access to such RF-ready design tools, designers are hard pressed to design products that meet the tight constraints on power consumption and noise. These constraints leave very little margin for error.

This paper describes an approach to make design tools RF-ready through the use of better models that describe the high-frequency behavior of CMOS transistors. These models can be readily used in Spice simulators, the backbone of any physical design flow. In essence, these RF models are the enablers of CMOS RF designs.

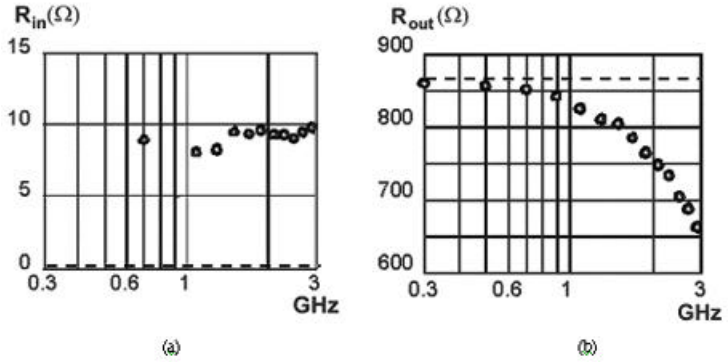
The organization of this paper is as follows. Section II describes the requirements of building an RF

CMOS model, where the concept of a subcircuit model is introduced. Section III outlines the modeling methodology and emphasizes model parameter extraction and optimization issues. Section IV provides design results. The conclusion, Section V, provides an outlook on the future of RF CMOS modeling.

RF CMOS MODEL REQUIREMENTS

Figures 2a and 2b demonstrate the importance of generating RF CMOS models. In these figures, simulation results from traditional low-frequency (typically, below 100 MHz) Spice models are compared to high-frequency measurement results. We can readily see how modeling accuracy (i.e.,, fit between simulated and measured data) starts to degrade for small-signal input and output resistances beyond 1 GHz.

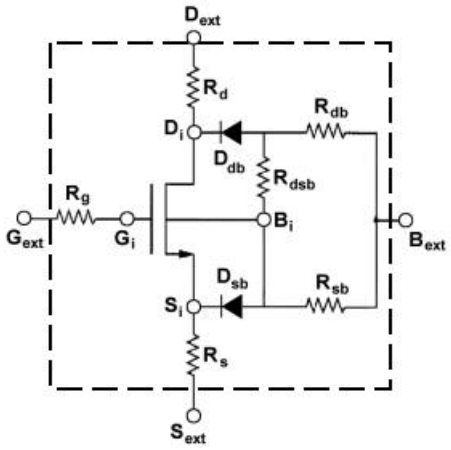
Figure 2. Low frequency DC models (dashed lines) cannot fit measured data (symbols) for input (a) and output (b) resistances in the gigahertz ranges.



The original formulation of low-frequency Spice models is responsible for this poor modeling of high-speed characteristics. Spice models were developed for digital and analog circuits, where emphasis is placed on dc drain current, conductances and intrinsic charge/capacitance behavior in the megahertz range. However, as applications are now demanding gigahertz frequencies, the importance of extrinsic components has steadily gained ground and has come to rival that of their intrinsic counterparts. One example of such a component is substrate resistance. At gigahertz frequencies, signals at the drain of the MOSFET can couple to the substrate and source as a result of the decrease in impedance of the junction capacitances.

Because of this coupling and other physical effects, certain external elements need to be attached to the intrinsic nodes of a MOSFET as shown in Figure 3. The process of extracting these external values to fit measured RF characteristics while still ensuring good dc and ac (i.e.,, low-frequency) fitting results constitutes an RF CMOS modeling methodology. The implementation of such a methodology is described in Section III.

Figure 3. Various external elements are attached to the intrinsic MOSFET (with its terminals subscripted by i) to constitute a 'sub-circuit,' which is outlined by the dashed box. An RF CMOS modeling flow extracts the parameters for the elements within this box.



In addition to extracting parameters for external elements, various other physical effects need to be modeled to ensure proper description of all high-frequency effects. The first of these is thermal noise. Thermal noise comprises three parts: noise from Rg (i.e.,, gate resistance), noise from the extrinsic physical resistances (i.e.,, Rd, Rs, Rdb, Rsb and Rdsb) and channel thermal noise. The last is the dominant noise source and must be carefully modeled. This requires modifications to the intrinsic MOSFET model such as those proposed by BSIM4[1]. Adding extrinsic elements will not solve the problem.

The second physical phenomenon commonly seen in RF designs is referred to as the Non-Quasi Static (NQS) effect. This effect occurs when the MOSFET's operation frequency approaches that of the unity gain, ft. This is a reference frequency and is defined to be the point at which the small-signal current gain equals 1. Figure 1 shows that the ft for modern CMOS transistors is approximately 30 GHz. Thus, as the frequency approaches and surpasses ft the time required to charge and discharge the intrinsic capacitances becomes non-negligible in comparison to the operating frequencies. So traditional analysis techniques that use small-signal equivalent circuits (see Section IIIB) begin to unravel. One way to remedy this effect is to replace every intrinsic capacitance with an RC series network. While this appears effective, it requires substantial revisions to the intrinsic core of the MOSFET model.

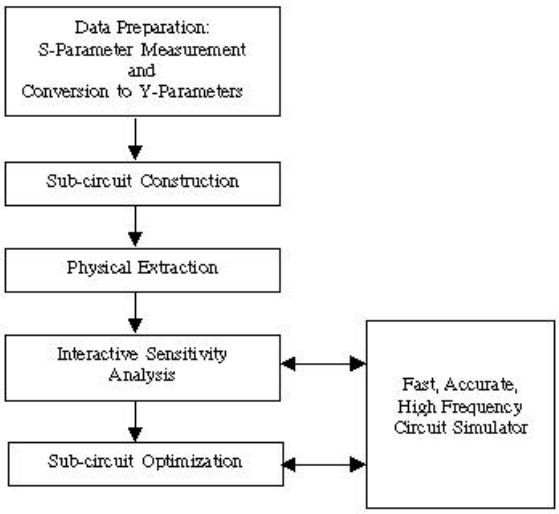
The last effect, which is very important to RF designs, is the problem of large-signal modeling or distortion. In RF design, when a sinusoidal input signal is applied to the gate of a MOSFET the output drain signal can contain not only the input frequency (i.e.,, ground harmonic) but higher order harmonics as well. The cause of distortion is due to the nonlinearity of MOSFET drain current and capacitance characteristics. Thus, in order to model distortion effects well we must accurately model the higher order derivatives of the drain current and capacitance.

This paper tackles the issue of extracting model parameter values for the subcircuit in Figure 3. The purpose is to provide a modeling flow to fit a MOSFET's small-signal behavior at RF frequencies. Problems of thermal noise, NQS and large signal behaviors are not included as they require substantial revisions to the intrinsic MOSFET model core. These revisions are beyond the scope of model extraction and border on the formulation of a completely different compact Spice model.

RF CMOS MODELING METHODOLOGY

Figure 4 describes an RF CMOS modeling flow. Each of its elements is described below.

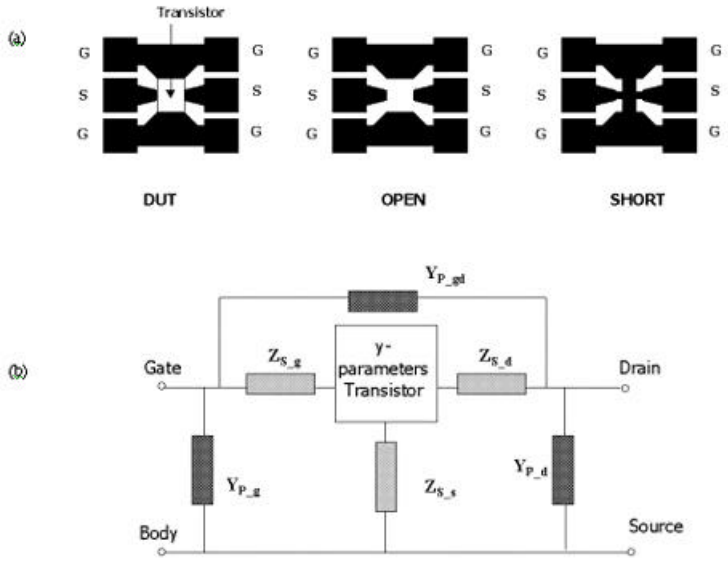
Figure 4. The main steps in an RF CMOS modeling flow must include physical extraction in order to reduce optimization time as simulating the sub-circuit can take particularly long



Data Preparation: The use of s-parameters for RF CMOS modeling is not new, and the basic advantages of measuring them still apply. At RF microwave frequencies, the ability to make precise measurements on the MOSFET transistor without lead inductance and fringing capacitance is a real concern. This can be exacerbated if the measurement scheme in question requires open and short-circuit signal conditions, which are difficult to maintain under high-frequency operations. With s-parameter measurement, there is no need to uphold such a criterion. Rather, s-parameter measurements operate on the theory of matched loads. We will not dwell upon the theoretical underpinnings of s-parameters here. Instead, interested readers should consult various references such as [2] for a more thorough treatment of the subject.

Measurements made using s-parameters must go through a de-embedding process. This is largely because the measured data contains parasitics brought about by the test structure itself. Things such as pad and metal line parasitics must be removed before the data can be used for modeling. Figure 5a shows an example of the open and short test structures involved. Data collected from the open one mainly suffers from parallel parasitics. The data from the shorted test structure suffers from both parallel and series parasitics. Thus, open and short test structures can be used in tandem to calculate the separate contribution of parallel and series parasitics. These can then be used to de-embed (Figure 5b) all parasitics from the data measured using the device under test (DUT) test structure. One proposed method [3] is shown in Equation 1. The properly de-embedded data will be used in the remainder of the RF CMOS extraction flow.

Figure 5. Two test structures (an Open and Short structure) are included (a) to de-embed the data collected from the DUT. Open test structure contributes to parallel parasitics and is denoted by parallel Y elements (b). Short test structures have both parallel and series parasitics but can be graphically denoted by the series Z elements.



It is important to understand that the s-parameter measurements are small-signal measurements, so they lend themselves well to traditional small-signal equivalent circuit analysis. For s-parameter data to be used in this way, it must first be converted into an alternative representation; the most commonly used are y-parameters. This conversion is performed through a fixed set of equations [4]. Besides their physical meaning (i.e.,, y-parameters are referred to as admittance, or the inverse of impedance), y-parameter data also has very smooth characteristics, important attributes that can be exploited during subcircuit optimization, the subject of Section IIID.

$$[Y_{Device}] = (([Y_{DUT}] - [Y_{Dummy\_open}]^{-1}) - [Y_{Dummy\_short}] - [Y_{Dummy\_open}])^{-1})^{-1}$$

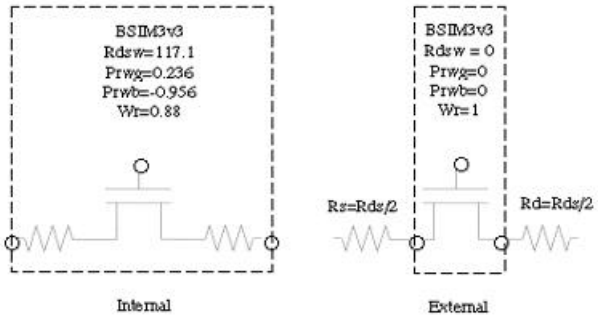
Subcircuit construction: As previously mentioned, the subcircuit of Figure 3 can be used to represent certain extrinsic effects at high frequencies. It is important to note that the subcircuit model and its extracted parameters are meant to fit measured y-parameters for a single device with multiple bias conditions. However, this fitting must be achieved while still maintaining good dc and low-frequency fitting accuracy. This can place additional considerations on the subcircuit construction process. In order to make the methodologies we present in this paper applicable to real-world design, we will construct a subcircuit using the BSIM3v3 Spice model, the industry de facto standard intrinsic MOSFET model, to illustrate the problems and provide solutions.

$$Rds = \frac{Rdsw[1 + Prwg\ Vgsteff + Prwb(\sqrt{\phi_s - Vbseff} - \sqrt{\phi_s})]}{(10^6\ Weff')^{Wr}}$$

The addition of external source and drain resistances poses a dilemma for simultaneous fitting of dc and RF measured data. Simply adding two additional resistors will likely worsen dc fitting characteristics (i.e.,, introduce additional voltage drop at the terminals). Yet by defining two external resistances, we can have more freedom to fit y-parameter data and also allow the external junction diodes to be attached to the intrinsic source and drains. This is desirable from an accuracy point of view. One solution would be to use the original BSIM3v3 model parameter and set it to calculate the external values of Rd and Rs (Equation 2). External resistances equal to these calculated values are attached to the intrinsic drain and source nodes, respectively. At the same time, all model parameters related to intrinsic drain/source resistance calculation should be turned off (Figure 6). Another method would be to perform dc model extraction with external resistances (i.e.,, internal resistance model parameters must be turned off) from the start. Although this appears to require more effort it is the best approach for satisfying both dc and RF modeling needs.

Figure 6. Transferring source/drain resistances from internal to external resistances. BSIM3v3 Rds related model parameters are then disabled. The dashed lines represent

MOSFET model description.



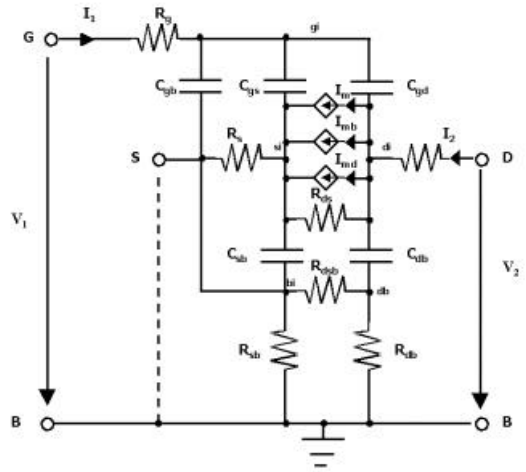
Besides external source/drain resistances, an external gate resistance is needed. This resistor not only represents the physical gate electrode resistance but also the resistance of the channel as seen from the gate. Physical gate resistance scales with the inverse of channel length, L (i.e.,, as L increases, the physical gate resistance decreases). The channel resistance was found to have bias (i.e.,, Vgs and Vds) and channel length dependencies [5]. Since our subcircuit is meant to fit one device, the channel length dependence can be temporarily ignored. The resulting bias dependencies can be implemented with a voltage-controlled resistor.

External diodes are needed to model the coupling from source/drain to the body. Once these external diodes are used in the subcircuit, the built-in junction diodes in BSIM3v3 must be turned off. The best way to do this is to set all the area and perimeter calculation coefficients to zero.

The last items to be added are the resistances in the substrate. Various publications have individually touted physical basis for either one [6] or four [7] individual resistors. The tradeoff is always between additional degrees of freedom afforded by the extra resistors during optimization and the extended optimization time. We recommend the three-resistor network as shown in Figure 3.

Physical extraction: The purpose of physical extraction is to provide a good initial guess for the subsequent optimization of the external model parameters of Figure 3. To carry out this extraction process, the technique from [8, 9] is used with some modifications. The subcircuit of Figure 3 is realized as a two-port y-parameter network. Its small-signal equivalent circuit (Figure 7) is then used to derive mathematical expressions for the four parameters y11, y12, y21 and y22.

Figure 7. The small-signal equivalent circuit of Figure 3 is shown in a 2-port network configuration. This circuit is used to derive mathematical expression for y-parameters. These will then be used in extraction.



These expressions, hence, relate measurable quantities (i.e., the y-parameters) to the extrinsic elements. Equation 3 shows one example of such an expression for the y11 parameter. This expression is derived when the two-port is measured with a Vds=0 V bias.

$$y_{11} \cong j\omega C_{gg} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d)$$

where, . Parameters can then be extracted by:

where, $C_{gg} = C_{gd} + C_{gs} + C_{gb}$. Parameters can then be extracted by:

$$C_{gg} = \left| \frac{\mathrm{Im}(y_{11})}{\omega} \right|$$

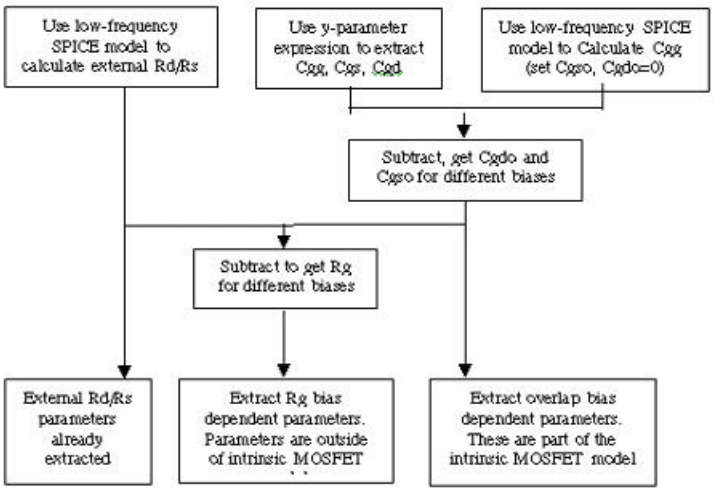
Other parameters can use mathematical derivations for the other y-parameters such as:

$$C_{gd} = \left| \frac{\mathrm{Im}(y_{12})}{\omega} \right|$$

Thus, physical extraction is a mathematical calculation and does not involve numerous iterations. Its accuracy is limited by the assumptions used to derive its mathematical expressions. Such assumptions are necessary in order to maintain simplicity and usefulness.

Our proposed extraction flow is shown in Figure 8. This flow extracts all extrinsic parameters except those within the substrate network. These substrate resistance values are best extracted using optimization because of the complexity of the resistance network. Note that the extraction flow begins with using gate capacitance and transcapacitances to extract gate resistance and overlap capacitance terms. These latter two physical quantities are essential in producing good-fitting results.

Figure 8. Physical extraction flow extracts extrinsic (Rg, Rd, and Rs) model parameters as well as intrinsic ones (overlap capacitances).



Sensitivity analysis and optimization: Some of the previous model parameter values determined by physical extraction can be changed (only slightly, it's hoped) in order to achieve even better fitting accuracy between measured and simulated y-parameter characteristics. This optimization process provides a unique challenge to RF CMOS model extraction because of the subcircuit nature of the model. The introduction of so many extrinsic elements really means that we are optimizing a circuit (albeit a small one) in contrast to a single device used in traditional low-frequency modeling. This places high-speed requirements on the circuit simulator, which by default is of the Spice variety--not known for speedy calculations.

A better approach is to consider the optimization problem in a slightly different manner. Optimization is essentially a simulation-intensive procedure. Thus, any method that can reduce

simulation time can ultimately improve optimization speeds. As mentioned in Section IIIA, the smooth, monotonic behavior of y-parameters can potentially be applied in just such a scenario. Because of this fact, it is not necessary to simulate and optimize every measured bias point. Mathematical functions can be used to link the many bias points. This allows accurate prediction of overall trends through the simulation of a subset of the original bias points. For example, if every tenth data point is used, then the simulation time will be greatly reduced by one order of magnitude.

A fast simulation algorithm is beneficial not just from a pure optimization point of view. It can also help in deciding which model parameters should be selected for optimization. Interactive Sensitivity Analysis allows model parameter values to be changed so that the resulting effect on y-parameters characteristics of the entire subcircuit to be seen in real time. This feature can help to zero in on the most sensitive set of parameters, thereby reducing the optimization time. Table 1 lists a recommended collection of parameters that can be optimized and their intended targets.

Table 1. Different model parameters can be used to fit different y-parameters.

Parameter to be Optimized	Fitting Target
R_g	$Re(y_{11})$
R_{dsb}, R_{sb}, R_{db}	$Re(y_{22})$ and $Im(y_{22})$
C_{gso}	$Im(y_{11})$
C_{gdo}	$Im(y_{12})$, $Im(y_{21})$
C_{gbo}	$Im(y_{11})$, $Im(y_{12})$, $Im(y_{21})$

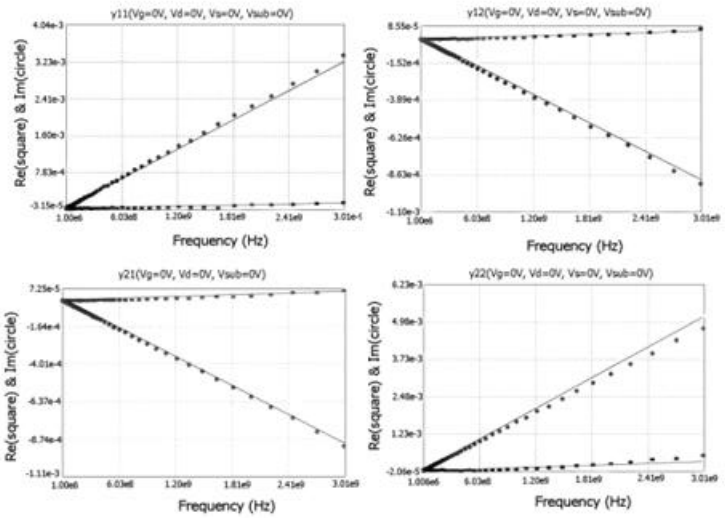
Table 2. Overall RMS errors are an average of RMS errors for Real and Imaginary y-parameter data.

Bias Condition	Overall RMS Fitting Error (%)			
	y_{11}	y_{12}	y_{21}	y_{22}
(Vgs=0, Vds=0, Vbs=0)	2.92	1.88	2.45	3.11
(Vgs=0, Vds=3, Vbs=0)	1.23	0.98	0.67	2.13
(Vgs=0.8, Vds=0, Vbs=0)	0.95	5.40	5.16	23.12
(Vgs=0.8, Vds=3, Vbs=0)	0.73	1.73	0.35	2.58

RESULTS

Figures 9a through 9d show the fitting for an n-MOS 10 um/0.35 um transistor with 20 fingers (effectively a 200 um/0.35 um device). Good agreement with measured y-parameter data is seen for all four y-parameters. Table 2 shows a low RMS fitting error across all four different bias conditions. The extracted subcircuit model can now be used for RF CMOS designs, thus obviating the need to perform handle calculations and pad design margins.

Figure 9. Good fit can be seen for all y-parameters. The good fit of y11 ensures good fit of Rin (=Re[1/y11]). The good fit of y22 ensures good fit of Rout (=Re[y22]).



There is little doubt that wireless applications will continue to drive the development of integrated low-cost CMOS products. An accurate and practical RF CMOS modeling methodology is one of the crucial elements for ensuring a successful design. This paper introduced such a methodology. It is practical in that it uses an industry de facto standard model as its basis. It is accurate because it makes provisions for maintaining low-frequency fitting results while providing good high-frequency modeling accuracy. Future implementations of this methodology will have to consider additional effects such as thermal noise, nonquasi static effects and large signal modeling.

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