BSIM3v3 Manual

(Final Version)

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How to get a copy of this manual and SPICE source code (model part only):

anonymous ftp site: rely.eecs.berkeley.edu or 128.32.156.10

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CHAPTER 1: Introduction

1.1 General Information

BSIM3v3 is the latest physics-based, deep-submicron MOSFET model for digital and analog circuit designs from the Device Group at the University of California at Berkeley. BSIM3v3 has been extensively modified from its previous release (BSIM3 Version 2.0). Amongst the new advancements are:

- A single I-V expression to describe current and output conductance characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions. Such a formulation guarantees the continuities of Ids, Gds, Gm and their derivatives throughout all Vgs, Vds and Vbs bias conditions. In addition, all previous kinks and glitches at device operation boundaries are eliminated.
- New width dependencies for bulk charge and source/drain resistance (Rds). This greatly enhances the accuracy in modeling narrow width devices.
- ΔW and ΔL dependencies for different Wdrawn and Ldrawn devices. This improves the model's ability to fit a variety of W/L ratios with a single set of parameters.
- A new capacitance model has been formulated to address the concern and to improve the modeling of short and narrow geometry devices.
- Lastly, BSIM3v3 includes a new relaxation time model for characterizing the non-quasi-static effect of MOS circuits for improved transient modeling.

In the mist of all these new features, BSIM3v3 still retains the same physical underpinnings of BSIM3 Version 2.0. For example, his new model still has the extensive built-in dependencies of important dimensional and processing parameters (e.g. channel length, width, gate oxide thickness, junction depth, substrate doping concentration, etc.). This allows users to accurately model the MOSFET over a wide range of channel lengths as well as channel widths for present as well as future technologies. Furthermore, BSIM3v3 still relies on a coherent pseudo-2D formulation to model various short-channel and high field effects such as the following:

- threshold voltage roll-off,
- non-uniform doping effect,
- mobility reduction due to vertical field,
- carrier velocity saturation,
- channel-length modulation,
- drain induced barrier lowering,
- substrate current-induced body effect,
- subthreshold conduction, and
- parasitic resistance effect.

Meticulous care has been taken to mesh the above model enhancements with high levels of accuracy and minimum simulation costs. In addition, the enhanced expressions yield more continuous behavior and should also help to facilitate faster SPICE convergence properties.

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1.2 Organization of Manual

The manual will introduce BSIM3v3's capabilities in the following manner:

- Chapter 2 will highlight the physical basis and arguments used in deriving BSIM3v3's I-V equations.
- Chapter 3 will combine these various BSIM3v3 equations for different operational regimes in a unified I-V model.
- Chapter 4 will present the new capacitance model.
- Chapter 5 will detail the inclusion of the new model for transient modeling called the NQS (Non-Quasi-Static) Model.
- Chapter 6 will discuss SPICE model file extraction.
- Chapter 7 will provide results of some benchmark tests applied on the model to illustrate its general robustness (no discontinuities).
- Chapter 8 will conclude with the noise model.
- Chapter 9 will describe the MOS diode model.
- Finally, the Appendix will list all model equations and references used throughout this manual. In addition, model parameters which can be binned during parameter extraction will also be listed.

CHAPTER 2: Physics-Based Derivation of the I-V Model

BSIM3v3's development is based upon finding solutions to Poisson's equation using Gradual Channel Approximation (GCA) and Quasi-Two Dimensional Approximation (QTDA) approaches. It includes compact, analytical expressions for the following physical phenomenon observed in present day MOS devices [1]:

- Short and narrow channel effects on threshold voltage.
- Non-uniform doping effect (in both lateral and vertical directions).
- Mobility reduction due to vertical field.
- Bulk charge effect.
- Carrier velocity saturation.
- Drain-induced barrier lowering (*DIBL*).
- Channel length modulation (*CLM*).
- Substrate current induced body effect (*SCBE*).
- Subthreshold conduction.
- Source/drain parasitic resistances.

2.1 Non-Uniform Doping and Small Channel Effects on Threshold Voltage

Accurate modeling of threshold voltage (Vth) is one of the most important requirements for the precise description of a device's electrical characteristics. In addition, it serves as a useful reference point for the evaluation of device operation

regimes. By using threshold voltage, the whole device operation regime can be divided into three operational regions.

First, if the gate voltage is greater than the threshold voltage, the inversion charge density is larger than the substrate doping concentration. The MOSFET is then operating in the strong inversion region and drift current is dominant. Second, if the gate voltage is much less than the threshold voltage, the inversion charge density is smaller than the substrate doping concentration. The MOSFET is now considered to be operating in the weak inversion (or subthreshold) region. Diffusion current is now dominant [2]. Lastly, if the gate voltage is very close to the threshold voltage, the inversion charge density is close to the doping concentration and the MOSFET is operating in the transition region. In such a case, both diffusion and drift currents are equally important.

The standard threshold voltage of a MOSFET with long channel length/width and uniform substrate doping concentration [2] is given by:

$$V_{th} = V_{FB} + \phi_s + \gamma\sqrt{\phi_s - V_{bs}} = V_{Tideal} + \gamma(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) \tag{2.1.1}$$

where V_{FB} is the flat band voltage, V_{Tideal} is the ideal threshold voltage of the long channel device at zero volt substrate bias, and γ is the substrate bias effect coefficient and is given by:

$$\gamma = \frac{\sqrt{2\varepsilon_{si} q N_a}}{C_{ox}} \tag{2.1.2}$$

where N_a is the substrate doping concentration. The surface potential is given by:

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$$\phi_s = 2\frac{K_B T}{q}\ln(\frac{N_a}{n_i}) \tag{2.1.3}$$

Equation (2.1.1) assumes that the channel is uniform and makes use of the one dimensional Poisson equation in the vertical direction of the channel. This model is valid only when the substrate doping concentration is constant and the channel length is long. Under these conditions, the potential is uniform along the channel. But in reality, these two conditions are not always satisfied. Modifications have to be made when the substrate doping concentration is not uniform or and when the channel length is short, narrow, or both.

2.1.1 Vertical Non-Uniform Doping Effect

The substrate doping level is not constant in the vertical direction as shown in Figure 2-1.

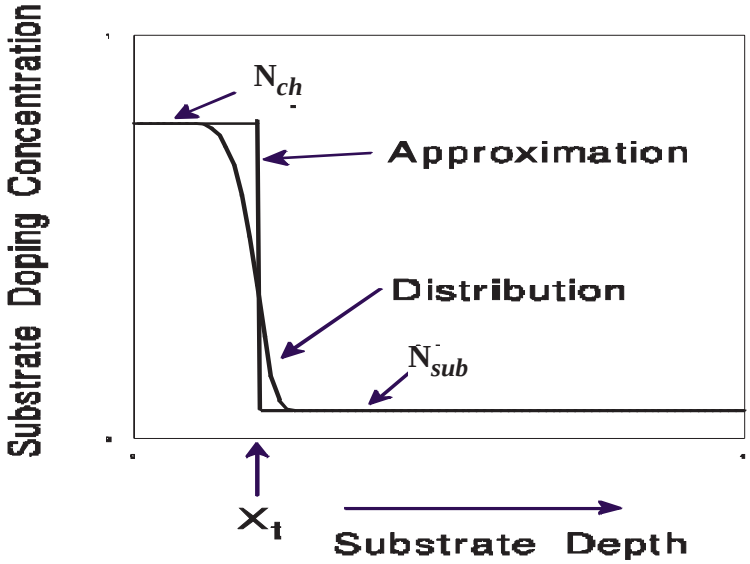

Figure 2-1. Actual substrate doping distribution and its approximation.

The substrate doping concentration is usually higher near the silicon to silicon dioxide interface (due to the threshold voltage adjust implant) than deep into substrate. The distribution of impurity atoms inside the substrate is approximately a half gaussian distribution, as shown in Figure 2-1. This non-uniformity will make γ in Eq. (2.1.2) a function of the substrate bias. If the depletion width is less than X_t as shown in Figure 2-1, N_a in Eq. (2.1.2) is equal to N_{ch}, otherwise it is equal to N_{sub}.

In order to take into account such non-uniform substrate doping, the following threshold voltage model is proposed:

$$V_{th} = V_{Tideal} + K_1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K_2 V_{bs} \tag{2.1.4}$$

For a zero substrate bias, Eqs. (2.1.1) and (2.1.4) give the same result. K_1 and K_2 can be determined by the criteria that V_{th} and its derivative versus V_{bs} should be the same at V_{bm}, where V_{bm} is the maximum substrate bias voltage. Therefore, using equations (2.1.1) and (2.1.4), K_1 and K_2 [3] will be given by the following:

$$K_1 = \gamma_2 - 2K_2\sqrt{\phi_s - V_{bm}} \tag{2.1.5}$$

$$K_2 = (\gamma_1 - \gamma_2)\frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}} \tag{2.1.6}$$

where γ_1 (or γ_2) is the body effect coefficient when the substrate doping concentration is N_{ch} (or N_{sub}) as shown in Figure 2-1.

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$$\gamma_1 = \frac{\sqrt{2q\varepsilon_{si}N_{ch}}}{C_{ox}} \tag{2.1.7}$$

$$\gamma_2 = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}} \tag{2.1.8}$$

V_{bx} is the body bias when the depletion width is equal to X_t. Therefore, V_{bx} satisfies:

$$\frac{qN_{ch}X_t^2}{2\varepsilon_{si}} = \phi_s - V_{bx} \tag{2.1.9}$$

If the devices are available, K_1 and K_2 can be determined experimentally. If the devices are not available but the user knows the doping concentration distribution, the user can input the appropriate parameters to specify doping concentration distribution (e.g. N_{ch}, N_{sub}, X_t). Then, K_1 and K_2 can be calculated using equations (2.1.5) and (2.1.6).

2.1.2 Lateral Non-Uniform Doping Effect:

For some technologies, the doping concentration near the drain and the source is higher than that in the middle of the channel. This is referred to as lateral non-uniform doping and is shown in Figure 2-2. As the channel length becomes shorter, lateral non-uniform doping will cause the threshold voltage to increase in magnitude because the average doping concentration in the channel is larger. The average channel doping can be calculated as follows:

$$N_{eff} = \frac{N_a(L-2L_x)+N_{ds}\cdot 2L_x}{L} = N_a(1+\frac{2L_x}{L}\frac{N_{ds}-N_a}{N_a}) \equiv N_a(1+\frac{Nlx}{L}) \tag{2.1.10}$$

Due to this lateral non-uniform doping effect, Eq. (2.1.4) becomes:

$$V_{th} = V_{tho} + K_1(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}) - K_2 V_{bs} + K_1\left(\sqrt{1+\frac{N_{LX}}{L_{eff}}}-1\right)\sqrt{\Phi_s} \tag{2.1.11}$$

Eq. (2.1.11) can be derived by setting $V_{bs} = 0$, and using $K_1 \propto (N_{eff})^{0.5}$. The fourth term in Eq. (2.1.11) is used empirically to model the body bias dependence of the lateral non-uniform doping effect. This effect gets stronger at a lower body bias. Examination of Eq. (2.1.11) shows that the threshold voltage will increase as channel length decreases [3].

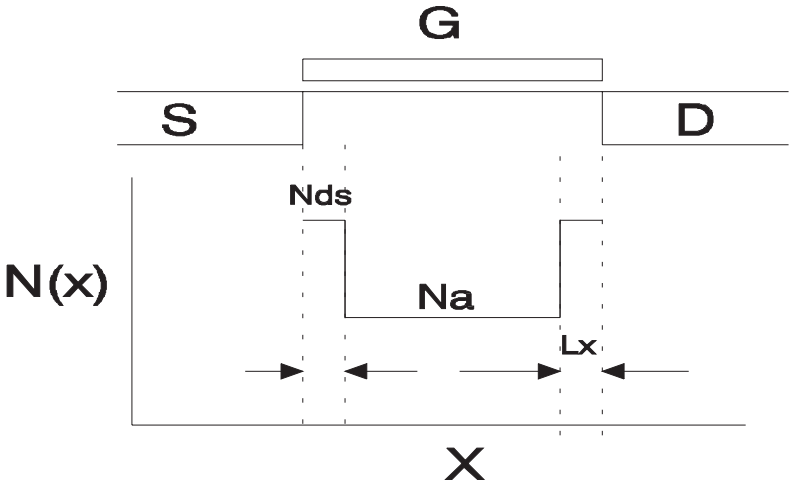

Figure 2-2. Doping concentration along the channel is non-uniform.

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2.1.3 Short Channel Effect

The threshold voltage of a long channel device is independent of the channel length and the drain voltage. Its dependence on the body bias is given by Eq. (2.1.4). However, as the channel length becomes shorter and shorter, the threshold voltage shows a greater dependence on the channel length and the drain voltage. The dependence of the threshold voltage on the body bias becomes weaker as channel length becomes shorter, because the body bias has less control of the depletion region. Short-channel effects must be included in the threshold voltage in order to model deep-submicron devices correctly.

The short channel effect can be modeled in the threshold voltage by the following:

$$V_{th} = V_{tho} + K_1(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}) - K_2 V_{bs} + K_1\left(\sqrt{1+\frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} \; - \Delta V_{th} \tag{2.1.12}$$

where ΔV_{th} is the threshold voltage reduction due to the short channel effect. Many models have been developed to calculate ΔV_{th}. They used either numerical solutions [4], a two-dimensional charge sharing approach [5,6], or a simplified Poisson's equation in the depletion region [7-9]. A simple, accurate, and physical model was developed by Z.H. Liu, et al, [10]. Their model was derived by solving the quasi two-dimension Poisson equation along the channel. This quasi-2D model concluded that:

$$\Delta V_{th} = \theta_{th}(L)[2(V_{bi} - \phi_s) + V_{ds}] \tag{2.1.13}$$

where V_{bi} is the built-in voltage of a PN junction between the substrate and the source. V_{bi} is given by:

$$V_{bi} = \frac{K_B T}{q} \ln\left(\frac{N_{ch} N_d}{n_i^2}\right) \tag{2.1.14}$$

where N_d in Eq. (2.1.14) is the source doping concentration, and N_{ch} is the substrate doping concentration. The expression $\theta_{th}(L)$ is a short channel effect coefficient that has a strong dependence on the channel length and is given by:

$$\theta_{th}(L) = [\exp(-L/2l_t) + 2\exp(-L/l_t)] \tag{2.1.15}$$

l_t is referred to as the "characteristic length" and is given by:

$$l_t = \sqrt{\frac{\varepsilon_{si} T_{ox} X_{dep}}{\varepsilon_{ox} \eta}} \tag{2.1.16}$$

X_{dep} is the depletion width in the substrate and is given by:

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\phi_s - V_{bs})}{qN_{ch}}} \tag{2.1.17}$$

X_{dep} is larger near the drain than in the middle of the channel due to the drain voltage. X_{dep} / η represents the average depletion width along the channel.

Based on above discussion, the influences of drain/source charge sharing and DIBL effects to Vth are described by (2.1.15). However, in order to

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make the model fit a wide technology range, several parameters such as D_{vt0}, D_{vt2}, *Dsub*, *Eta0* and *Etab* are introduced, and the following modes are used in SPICE to account for charge sharing and the DIBL effects separately.

$$\theta_{th(L)} = D_{vt0}[\exp(-D_{vt1}L/2l_t) + 2\exp(-D_{vt1}L/l_t)] \tag{2.1.18}$$

$$\Delta V_{th(L)} = \theta_{th(L)}(V_{bi} - \phi_s) \tag{2.1.19}$$

$$l_t = \sqrt{\frac{\varepsilon_{si} T_{ox} X_{dep}}{\varepsilon_{ox}}}(1 + D_{vt2}V_{bs}) \tag{2.1.20}$$

$$\theta_{dibl(L)} = [\exp(-D_{sub}L/2l_{t0}) + 2\exp(-D_{sub}L/l_{t0})] \tag{2.1.21}$$

$$\Delta V_{th}(V_{ds}) = \theta_{dibl(L)}(E_{ta0} + E_{tab}V_{bs})V_{ds} \tag{2.1.22}$$

where l_{t0} is calculated by Eq. (2.1.20) at zero body-bias. D_{vt1} is basically equal to $1/(\eta)^{1/2}$ in Eq. (2.1.16). D_{vt2} is introduced to take care of the dependence of the doping concentration on substrate bias since the doping concentration is not uniform in the vertical direction of the channel. X_{dep} is calculated using the doping concentration in the channel (N_{ch}). D_{vt0}, D_{vt1},D_{vt2}, *Eta0*, *Etab* and *Dsub*, which are determined experimentally, can improve accuracy greatly. Even though Eqs. (2.1.18), (2.1.21) and (2.1.15) have different coefficients, they all still have the same functional forms. This the device physics represented by Eqs. (2.1.18), (2.1.21) and (2.1.15) are still the same.

As channel length L decreases, ΔV_{th} will increase, and in turn V_{th} will decrease. If a MOSFET has a *LDD* structure, N_d in Eq. (2.1.14) is the doping concentration in the lightly doped region. V_{bi} in a *LDD*-MOSFET will be smaller as compared to conventional MOSFETs, therefore the threshold voltage reduction due to the short channel effect will be smaller in *LDD*-MOSFETs.

As the body bias becomes more negative, the depletion width will increase as shown in Eq. (2.1.17). Hence ΔV_{th} will increase due to the increase in l_t. The term:

$$V_{Tideal} + K_1\sqrt{\phi_s - V_{bs}} - K_2 V_{bs}$$

will also increase as V_{bs} becomes more negative (for NMOS). Therefore, the changes in:

$$V_{Tideal} + K_1\sqrt{\phi_s - V_{bs}} - K_2 V_{bs}$$

and in ΔV_{th} will compensate for each other and make V_{th} less sensitive to V_{bs}. This compensation is more significant as the channel length is shortened. Hence, the V_{th} of short channel MOSFET is less sensitive to body bias as compared to a long channel MOSFET. For the same reason, the *DIBL* effect and the channel length dependence of V_{th} are stronger as V_{bs} is made more negative. This was verified by experimental data shown in Figure 2-3 and Figure 2-4. Although Liu, et al, found a accelerated V_{th} roll-off and non-linear drain voltage dependence [10] as the channel became very short, a linear dependence of V_{th} on V_{ds} is nevertheless a good approximation for circuit simulation as shown in Figure 2-4. This figure shows that Eq. (2.1.13) can fit the experimental data very well.

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Furthermore, Figure 2-5 shows how this model for V_{th} can fit various channel lengths under various bias conditions.

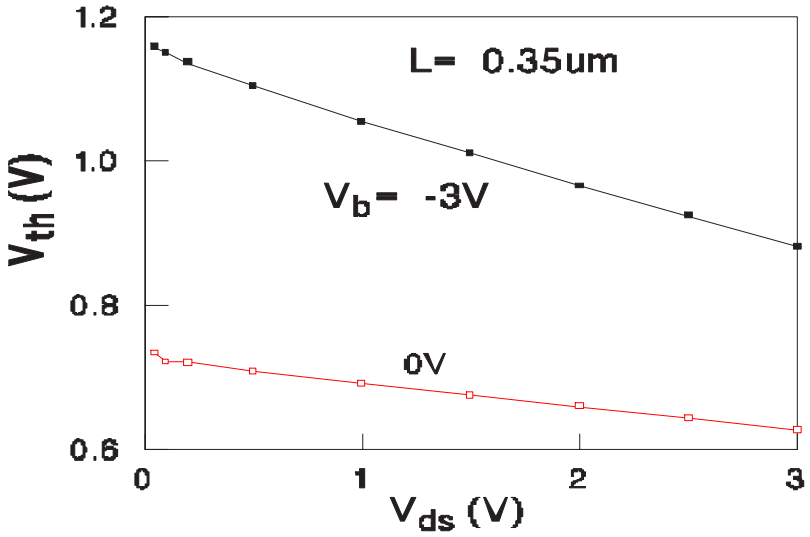

Figure 2-3. Threshold voltage versus the drain voltage at different body biases.

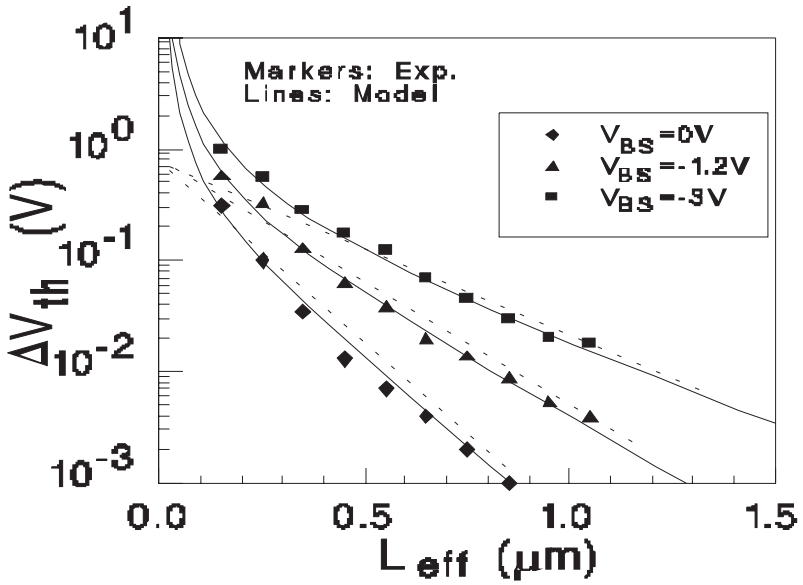

Figure 2-4. Channel length dependence of threshold voltage.

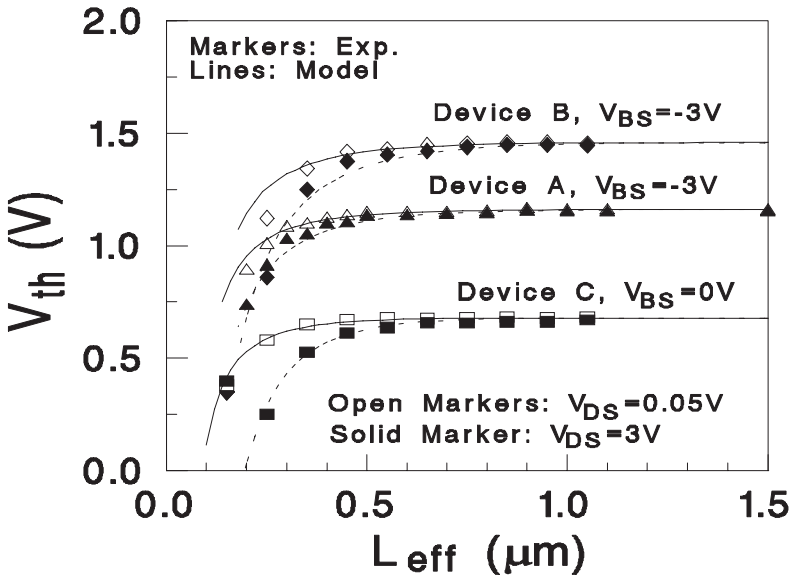

Figure 2-5. Threshold voltage versus channel length at different biases.

2.1.4 Narrow Channel Effect

The actual depletion region in the channel is always larger than what is usually assumed under the one-dimensional analysis due to the existence of fringing fields [2]. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the "classical" depletion layer formed from the vertical field. The net result is an increase threshold voltage magnitude. It is shown in [2] that this increase can be modeled as:

(2.1.23)

$$\frac{\pi q N_a (X_{d\max})^2}{2C_{ox}W} = 3\pi \frac{T_{ox}}{W}\phi_s$$

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The right hand side of Eq. (2.1.23) represents the additional voltage increase. BSIM3v3 models this change in threshold voltage by Eq. (2.1.24a). This formulation includes but is not limited to the inverse of channel width due to the fact that the overall narrow width effect is dependent on process (i.e. isolation technology) as well. Hence, the introduction of parameters K_3, K_{3b}, and W_0.

(2.1.24a)

$$(K_3 + K_{3b}V_{bs})\frac{T_{ox}}{(W_{eff}' + W_0)}\phi_s$$

W_{eff}' is the effective channel width (with no bias dependencies), which will be defined Section 2.9. In addition, we must also consider the narrow width effect for small channel lengths. To do this we introduce the following:

(2.1.24b)

$$D_{VT0w}\left(exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{2l_{tw}}) + 2exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{l_{tw}})\right)(V_{bi} - \Phi_s)$$

When all of the above considerations for non-uniform doping, short and narrow channel effects on threshold voltage are considered, the final, complete Vth expression implemented in SPICE is as follows:

(2.1.25)

$$\begin{aligned} V_{th} = {} & V_{tho} + K_1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K_2 V_{bseff} \\ & + K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff})\frac{T_{OX}}{W_{eff}' + W_0}\Phi_s \\ & - D_{VT0w}\left(exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{2l_{tw}}) + 2exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{l_{tw}})\right)(V_{bi} - \Phi_s) \\ & - D_{VT0}\left(exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)(V_{bi} - \Phi_s) \end{aligned}$$

(2.1.25) (cont.)

$$- \left(\exp(-D_{sub}\frac{L_{eff}}{2l_{to}}) + 2\exp(-D_{sub}\frac{L_{eff}}{l_{to}}) \right)(E_{tao} + E_{tab}V_{bseff})\,V_{ds}$$

In Eq. (2.1.25), all Vbs terms have been substituted with a Vbseff expression as shown in Eq. (2.1.26). This is done in order to set an upper bound for the body bias value during simulations. Unreasonable values can occur if this expression is not introduced. See Section 3.8 for details

(2.1.26).

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\ ]$$

where δ_1=0.001. The parameter *Vbc* is the maximum allowable V_{bs} value and is calculated from the condition of dV_{th}/dV_{bs}=0 for the V_{th} expression of 2.1.4, 2.1.5, and 2.1.6 is equal to:

$$V_{bc} = 0.9(\phi s - \frac{K1^2}{4K2^2})$$

2.2 Mobility Model

A good model for surface carrier mobility is very critical to the accuracy of a MOSFET model. The scattering mechanisms responsible for surface mobility basically include phonons, coulombic scattering sites, and surface roughness [11, 12]. For good quality interfaces, phonon scattering is generally the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on gate oxide thickness, doping concentration, threshold voltage, gate voltage and

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substrate voltage, etc. Sabnis and Clemens [13] proposed an empirical unified formulation based on the concept of an effective field E_{eff} which lumps many process parameters and bias conditions together. E_{eff} is defined by

$$E_{eff} = \frac{Q_B + (Q_n/2)}{\varepsilon_{si}} \tag{2.2.1}$$

The physical meaning of E_{eff} can be interpreted as the average electrical field experienced by the carriers in the inversion layer [14]. The unified formulation of mobility is then empirically given by:

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} \tag{2.2.2}$$

Values for μ_0, E_0, and ν were reported by Liang *et al*. [15] and Toh *et al*. [16] to be the following for electrons and holes:

Parameter	Electron (surface)	Hole (surface)
μ_0 *(cm²/V)*	670	160
E_0 *(MV/cm)*	0.67	0.7
ν	1.6	1.0

Table 2-1. Mobility and related parameters for electrons and holes.

For a NMOS transistor with n-type poly-silicon gate, Eq. (2.2.1) can be rewritten in a more useful form that explicitly relates E_{eff} to the device parameters [14]:

(2.2.3)

$$E_{eff} \cong \frac{V_{gs} + V_{th}}{6T_{ox}}$$

Eq. (2.2.2) fits experimental data very well [15], but it involves a power function which is a very time consuming function for circuit simulators such as SPICE. A Taylor expansion Eq. (2.2.2) is used, and the coefficients are left to be determined using experimental data or to be obtained by fitting the unified formulation. Thus, we have:

(Mobmod=1) (2.2.4)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gst} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gst} + 2V_{th}}{T_{OX}})^2}$$

where Vgst=Vgs-Vth. To account for depletion mode devices, another mobility model option is given by the following:

.(Mobmod=2) (2.2.5)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gst}}{T_{OX}}) + U_b(\frac{V_{gst}}{T_{OX}})^2}$$

The unified mobility expressions in subthreshold and strong inversion regions will be discussed in Section 3.2.

To consider the body bias dependence of Eq. 2.2.4 further, we have introduced the following expression:

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(For Mobmod=3) (2.2.6)

$$\mu_{eff} = \frac{\mu_o}{1 + [U_a(\frac{V_{gst} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gst} + 2V_{th}}{T_{OX}})^2](1 + U_c V_{bseff})}$$

2.3 Carrier Drift Velocity

Carrier drift velocity is one of the most important parameters that affects device performance characteristics. BSIM3v3 uses a simple and semi-empirical saturation velocity model [17] given by:

(2.3.1)

$$\begin{aligned} v &= \frac{\mu_{eff} E}{1 + (E/E_{sat})}, && E < E_{sat} \\ &= v_{sat}, && E > E_{sat} \end{aligned}$$

The parameter E_{sat} corresponds to the critical electrical field at which the carrier velocity becomes saturated. In order to have a continuous velocity model at $E = E_{sat}$, E_{sat} must satisfy:

(2.3.2)

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}$$

2.4 Bulk Charge Effect

When the drain voltage is large and/or when the channel length is long, the depletion "thickness" of the channel is not uniform along the channel length. This

will cause threshold voltage to vary along the channel. This effect is called bulk charge effect [14].

In BSIM3v3, the parameter $A_{bulk}$is used to take into account this bulk charge effect. This parameter is a modification from that of BSIM1 and BSIM2 where the bulk charge parameter was "*a*" [3]. Several extracted parameters such as A0, Bo,B1 are introduced to account for the channel length and width dependences of the bulk charge effect. In addition, the parameter *Keta* is introduced to model the change in bilk charge effect under high back or substrate bias conditions. It should be pointed out that narrow width effects have been considered in the formulation of Eq. (2.4.1). The A_{bulk} expression used in BSIM3v3 is given by:

(2.4.1)

$$A_{bulk} = (1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}[1 - A_{gs} V_{gsteff}(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}})^2] + \frac{B_o}{Weff' + B_1}\})\frac{1}{1 + K_{ETA} V_{bseff}}$$

where A_0, A_{gs}, K_1,B_o, B_1 and Keta are determined by experimental data. Eq. (2.4.1) shows that A_{bulk} is very close to *1.0* if the channel length is small, and A_{bulk} increases as channel length increases.

2.5 Strong Inversion Drain Current (Linear Regime)

2.5.1 Intrinsic Case (Rds=0)

In the strong inversion region, the general current equation at any point y along the channel is given by:

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$$I_{ds} = WC_{ox}(V_{gst} - A_{bulk}V_{(y)})v_{(y)} \tag{2.5.1}$$

The parameter $V_{gst} = (V_{gs} - V_{th})$, W is the device channel width, C_{ox} is the gate capacitance per unit area, V(y) is the potential difference between minority-carrier quasi-Fermi potential and the equilibrium Fermi potential in the bulk at point y, $v(y)$ is the velocity of carriers at point y, and A_{bulk} is the coefficient accounting for the bulk charge effect.

With Eq. (2.3.1) (i.e. before carrier velocity saturates), the drain current can be expressed as:

$$I_{ds} = WC_{ox}(V_{gs} - V_{th} - A_{bulk}V_{(y)})\frac{\mu_{eff}E_{(y)}}{1 + E_{(y)}/E_{sat}} \tag{2.5.2}$$

Eq. (2.5.2) can be rewritten as follows:

$$E_{(y)} = \frac{I_{ds}}{\mu_{eff}WC_{ox}(V_{gst} - A_{bulk}V_{(y)}) - I_{ds}/E_{sat}} = \frac{dV_{(y)}}{dy} \tag{2.5.3}$$

By integrating Eq. (2.5.3) from $y = 0$ to $y = L$ and $V(y) = V_s$ to $V(y) = V_d$, we arrive at the following:

$$I_{ds} = \mu_{eff}C_{ox}\frac{W}{L}\frac{1}{1 + V_{ds}/E_{sat}L}(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds} \tag{2.5.4}$$

The drain current model in Eq. (2.5.4) is valid before the carrier velocity saturates.

For instances when the drain voltage is high (and thus the lateral electrical field is high at the drain side), the carrier velocity near the drain saturates. The channel now can be reasonably divided into two portions: one adjacent to the source where the carrier velocity is field-dependent and the second where the velocity saturates. At the boundary between these two portions, the channel voltage is the saturation voltage (V_{dsat}) and the lateral electrical is equal to E_{sat}. After the onset of saturation, we can substitute $v = v_{sat}$ and $V_{ds} = V_{dsat}$ into Eq. (2.5.1) to get the saturation current:

$$I_{ds} = WC_{ox}(V_{gst} - A_{bulk}V_{dsat})v_{sat} \tag{2.5.5}$$

By equating eqs. (2.5.4) and (2.5.5) at $E = E_{sat}$ and $v_{ds} = V_{dsat}$, we can solve for saturation voltage V_{dsat}:

$$V_{dsat} = \frac{E_{sat}L(V_{gs} - V_{th})}{A_{bulk}E_{sat}L + (V_{gs} - V_{th})} \tag{2.5.6}$$

2.5.2 Extrinsic Case (Rds>0)

Parasitic source/drain resistance is an important device parameter which can affect MOSFET performance significantly. As a MOSFET's channel length scale down, the parasitic resistance will not be proportionally scaled. As a result, Rds will have a more significant on device characteristics. Model parasitic resistance in a direct method yields a complicated drain current expression. In order to make simulations more efficient, BSIM3v3 models parasitic resistances using simple expressions. The resulting drain current equation in the linear region can be calculate [3] as follows:

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(2.5.9)

$$I_{ds} = \frac{V_{ds}}{R_{tot}} = \frac{V_{ds}}{R_{ch} + R_{ds}}$$
$$= \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + V_{ds}/(E_{sat} L)} \frac{(V_{gst} - A_{bulk} V_{ds}/2) V_{ds}}{1 + R_{ds} \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_{gst} - A_{bulk} V_{ds}/2)}{1 + V_{ds}/(E_{sat} L)}}$$

Due to parasitic resistance, the saturation voltage V_{dsat} will be larger than that predicted by Eq. (2.5.6). Let Eq. (2.5.5) be equal to Eq. (2.5.9). The V_{dsat} with parasitic resistance R_{ds} expression is then:

(2.5.10)

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

The following are the expression for the variables *a*, *b*, and *c*:

(2.5.11)

$$a = A_{bulk}^2 R_{ds} C_{ox} W v_{sat} + (\frac{1}{\lambda} - 1) A_{bulk}$$
$$b = -(V_{gst}(\frac{2}{\lambda} - 1) + A_{bulk} E_{sat} L + 3 A_{bulk} R_{ds} C_{ox} W v_{sat} V_{gst})$$
$$c = E_{sat} L V_{gst} + 2 R_{ds} C_{ox} W v_{sat} V_{gst}^2$$
$$\lambda = A_1 V_{gst} + A_2$$

The last expression for λ is introduced to account for non-saturation effect of the device. In BSIM3v3, parasitic resistance is modeled as:

(2.5.11)

$$R_{ds} = \frac{R_{dsw}[1 + P_{r\,wg} V_{gsteff} + P_{r\,wb}(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})]}{(10^6 W_{eff}')^{Wr}}$$

The variable R_{dsw} is the resistance per unit width, *Wr* is a fitting parameter, P_{rwb} is the body effect coefficient, and P_{rwg} is the gate-bais effect effect.

2.6 Strong Inversion Current and Output Resistance (Saturation Regime)

A typical I-V curve and its output resistance are shown in Figure 2-6. Considering only the drain current, the I-V curve can be divided into two parts: the linear region in which the drain current increases quickly with the drain voltage and the saturation region in which the drain current has a very weak dependence on the drain voltage. The first order derivative reveals more detailed information about the physical mechanisms which are involved during device operation. The output resistance (which is the reciprocal of the first order derivative of the I-V curve) curve can be clearly divided into four regions in which have distinct R_{out} *vs.* V_{ds} dependences.

The first region is the triode (or linear) region in which carrier velocity is not saturated. The output resistance is very small because the drain current has a strong dependence on the drain voltage. The other three regions belong to the saturation region. As will be discussed later, there are three physical mechanisms which affect the output resistance in the saturation region: channel length modulation (*CLM*) [4, 14], drain-induced barrier lowering (*DIBL*) [4, 6, 14], and the substrate current induced body effect (*SCBE*) [14, 18, 19]. All three mechanisms affect the output resistance in the saturation range, but each of them dominates in only a single region. It will be shown next that channel length modulation (*CLM*)

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dominates in the second region, *DIBL* in the third region, and *SCBE* in the fourth region.

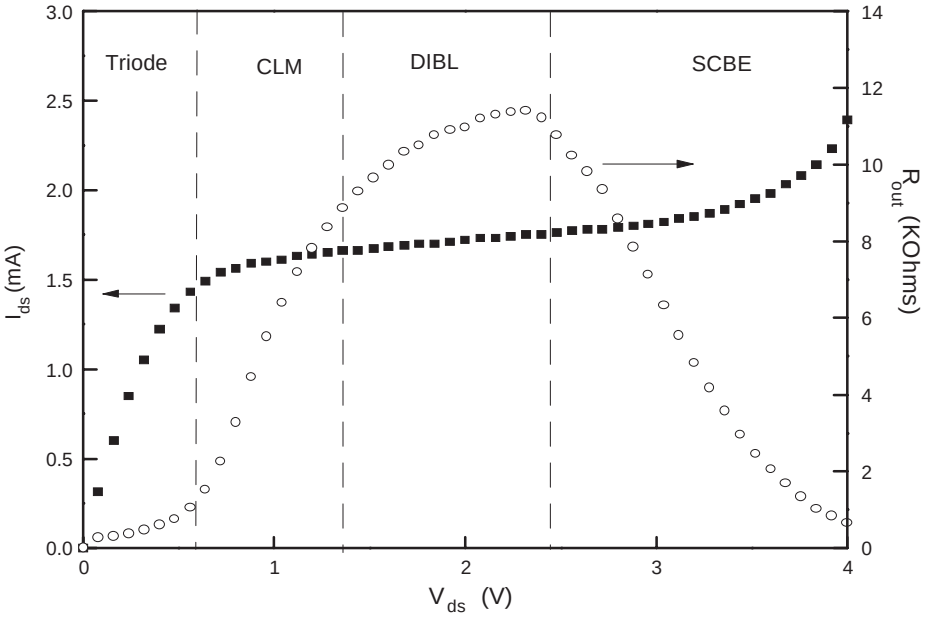

Figure 2-6. General behavior of MOSFET output resistance.

Generally, drain current is a function of the gate voltage and the drain voltage. But the drain current depends on the drain voltage very weakly in the saturation region. A Taylor series can be used to expand the drain current in the saturation region [3].

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{dsat}) + \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}}(V_{ds} - V_{dsat}) \tag{2.6.1}$$

$$\equiv I_{dsat}(1 + \frac{V_{ds} - V_{dsat}}{V_A})$$

where,

$$I_{dsat} = I_{ds}(V_{gs,}V_{dsat}) = Wv_{sat}C_{ox}(V_{gst} - A_{bulk}V_{dsat}) \tag{2.6.2}$$

and

$$V_A = I_{dsat}(\frac{\partial I_{ds}}{\partial V_{ds}})^{-1} \tag{2.6.3}$$

The parameter V_A is called the Early Voltage (analogous to the BJT) and is introduced for the analysis of the output resistance in the saturation region. Only the first order term is kept in the Taylor series. For simplicity, we also assume that the contributions to the Early Voltage from all three mechanisms are independent and can be calculated separately.

2.6.1 Channel Length Modulation (CLM)

If channel length modulation is the only physical mechanism to be taken into account, then according to Eq. (2.6.3), the Early Voltage can be calculated by:

$$V_{ACLM} = I_{dsat}(\frac{\partial I_{ds}}{\partial L}\frac{\partial L}{\partial V_{ds}})^{-1} = \frac{A_{bulk}E_{sat}L + V_{gst}}{A_{bulk}E_{sat}}(\frac{\partial \Delta L}{\partial V_{ds}})^{-1} \tag{2.6.4}$$

where ΔL is the length of the velocity saturation region, the effective channel length is L-ΔL. Based on the quasi-two dimensional approximation, V_{ACLM} can be derived as the following:

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L + V_{gst}}{A_{bulk}E_{sat}l}(V_{ds} - V_{dsat}) \tag{2.6.5}$$

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where V_{ACLM} is the Early Voltage due to channel length modulation alone.

The parameter P_{clm} is introduced into the V_{ACLM} expression not only to compensate for the error caused by the Taylor expansion in the Early Voltage model, but also to compensate for the error in X_j since:

$$l \propto \sqrt{X_j}$$

and the junction depth, X_j, can not generally be determined very accurately. Thus, the V_{ACLM} became:

$$V_{ACLM} = \frac{1}{P_{clm}} \frac{A_{bulk} E_{sat} L + V_{gst}}{A_{bulk} E_{sat} l} (V_{ds} - V_{dsat}) \tag{2.6.6}$$

2.6.2 Drain-Induced Barrier Lowering (DIBL)

As discussed above, threshold voltage is can be approximated as a linear function of the drain voltage. According to Eq. (2.6.3), the Early Voltage due to the *DIBL* effect can be calculated as:

$$V_{ADIBLC} = I_{dsat} \left(\frac{\partial I_{ds}}{\partial V_{th}} \frac{\partial V_{th}}{\partial V_{ds}} \right)^{-1} \tag{2.6.7}$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + P_{DIBLCB} V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t} \right)$$

During the derivation of Eq. (2.6.7), the parasitic resistance is assumed to be equal to 0. As expected, V_{ADIBLC} is a strong function of L as shown in Eq. (2.6.7). As channel length decreases, V_{ADIBLC} decreases very quickly.

The combination of the *CLM* and *DIBL* effects determines the output resistance in the third region, as was shown in Figure 2-6.

Despite the formulation of these two effects, accurate modeling of the output resistance in the saturation region requires that the coefficient $\theta_{th}(L)$ be replaced by $\theta_{rout}(L)$. Both $\theta_{th}(L)$ and $\theta_{rout}(L)$ have the same channel length dependencies, but different coefficients. The expression for $\theta_{rout}(L)$ *is:*

$$\theta_{rout}(L) = P_{diblc1}[\exp(-D_{rout}L / 2l_t) + 2\exp(-D_{rout}L / l_t)] + P_{diblc2} \tag{2.6.8}$$

The variables P_{diblc1}, P_{diblc2}, P_{diblcb} and D_{rout} are the newly introduced parameters to correct for DIBL effect in the strong inversion region. The reason why D_{vt0} is not equal to P_{diblc1} and D_{vt1} is not equal to D_{rout} is because the gate voltage modulates the *DIBL* effect. When the threshold voltage is determined, the gate voltage is equal to the threshold voltage. But in the saturation region where the output resistance is modeled, the gate voltage is much larger than the threshold voltage. Drain induced barrier lowering may not be the same at different gate bias. P_{diblc2} is usually very small (may be as small as *8.0E-3*). If P_{diblc2} is placed into the threshold voltage model, it will not cause any significant change. However it is an important parameter in V_{ADIBL} for long channel devices, because P_{diblc2} will be dominant in Eq. (2.6.8) if the channel is long.

2.6.3 Current Expression without Substrate Current Induced

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Body Effect

In order to have a continuous drain current and output resistance expression at the transition point between linear and saturation region, the V_{Asat} parameter is introduced into the Early Voltage expression. V_{Asat} is the Early Voltage at $V_{ds} = V_{dsat}$ and is as follows:

$$V_{Asat} = \frac{E_{sat}L + V_{dsat} + 2R_{ds}v_{sat}C_{ox}W(V_{gst} - A_{bulk}V_{ds}/2)}{1 + A_{bulk}R_{ds}v_{sat}C_{ox}W} \tag{2.6.9}$$

Thus, the total Early Voltage, V_A, can be written as:

$$V_A = V_{Asat} + (\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}})^{-1} \tag{2.6.10}$$

The complete (with no impact ionization at high drain voltages) current expression in the saturation region is given by:

$$I_{dso} = Wv_{sat}C_{ox}(V_{gst} - A_{bulk}V_{dsat})(1 + \frac{V_{ds} - V_{dsat}}{V_A}) \tag{2.6.11}$$

Furthermore, another parameter, P_{vag}, is introduced in V_A to account for the gate bias dependence of V_A more accurately. This much said, the final expression for Early Voltage becomes:

$$V_A = V_{Asat} + (1 + \frac{P_{vag}\tilde{V}_{gs}}{E_{sat}L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1} \tag{2.6.12}$$

2.6.4 Current Expression with Substrate Current Induced Body Effect

When the electrical field near the drain is very large (> 0.1MV/cm), some electrons coming from the source will be energetic (hot) enough to cause impact ionization. This creates electron-hole pairs when they collide with silicon atoms. The substrate current I_{sub} thus created during impact ionization will increase exponentially with the drain voltage. A well known I_{sub} model [20] is given as:

$$I_{sub} = \frac{A_i}{B_i} I_{dsat}(V_{ds} - V_{dsat}) \exp(-\frac{B_i l}{V_{ds} - V_{dsat}}) \tag{2.6.13}$$

The parameters A_i and B_i are determined from extraction. I_{sub} will affect the drain current in two ways. The total drain current will change because it is the sum of the channel current from the source as well as the substrate current. The total drain current can now be expressed [21] as follows:

$$\begin{aligned} I_{ds} &= I_{dso} + I_{sub} \\ &= I_{dso}\left[1 + \frac{(V_{ds} - V_{dsat})}{\frac{B_i}{A_i}\exp(\frac{B_i l}{V_{ds} - V_{dsat}})}\right] \end{aligned} \tag{2.6.14}$$

The total drain current, including *CLM*, *DIBL* and *SCBE*, can be written as:

$$I_{ds} = W v_{sat} C_{ox}(V_{gst} - A_{bulk} V_{dsat})(1 + \frac{V_{ds} - V_{dsat}}{V_A})(1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}}) \tag{2.6.15}$$

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where V_{ASCBE} can also be called as the Early Voltage due to the substrate current induced body effect. Its expression is the following:

$$V_{ASCBE} = \frac{B_i}{A_i}\exp(\frac{B_i l}{V_{ds} - V_{dsat}}) \tag{2.6.16}$$

From Eq. (2.6.16), we can see that V_{ASCBE} is a strong function of V_{ds}. In addition, we also observe that V_{ASCBE} is small only when V_{ds} is large. This is why *SCBE* is important for devices with high drain voltage bias. The channel length and gate oxide dependence of V_{ASCBE} comes from V_{dsat} and l. In BSIM3v3, we replace *Bi* with *PSCBE2* and *Ai/Bi* with *PSCBE1/L* to yield the following expression for V_{ASCBE}:

$$\frac{1}{V_{ASCBE}} = \frac{P_{SCBE2}}{L}\exp(-\frac{P_{SCBE1} l}{V_{ds} - V_{dsat}}) \tag{2.6.17}$$

The variables P_{scbe1} and P_{scbe2} are determined experimentally.

2.7 Subthreshold Drain Current

The drain current equation in the subthreshold region was given in [2, 3] can is expressed by the following:

$$I_{ds} = I_{s0}(1 - \exp(-\frac{V_{ds}}{v_t}))\exp(\frac{V_{gs} - V_{th} - V_{off}}{n v_t}) \tag{2.7.1}$$

(2.7.2)

$$I_{s0} = \mu_0 \frac{W}{L} \sqrt{\frac{q\varepsilon_{si} N_{ch}}{2\phi_s}} v_t^2$$

Here the parameter *vt* is the thermal voltage and is given by KBT/q. Voff is the offset voltage, as discussed in Jeng's dissertation [18]. Voff is an important parameter which determines the drain current at $V_{gs} = 0$. In Eq. (2.7.1), the parameter *n* is the subthreshold swing parameter. Experimental data shows that the subthreshold swing is a function of channel length and the interface state density. These two mechanisms are modeled in BSIM3v3 by the following:

(2.7.3)

$$n = 1 + N_{factor} \frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd} V_{ds} + C_{dscb} V_{bseff}) \left(\exp(-D_{VT1} \frac{L_{eff}}{2 l_t}) + 2 \exp(-D_{VT1} \frac{L_{eff}}{l_t}) \right)}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

where, the term:

$$(C_{dsc} + C_{dscd} V_{ds} + C_{dscb} V_{bseff}) \left(\exp(-D_{VT1} \frac{L_{eff}}{2 l_t}) + 2 \exp(-D_{VT1} \frac{L_{eff}}{l_t}) \right)$$

represents the coupling capacitance between the drain or source to the channel. The parameters Cdsc, Cdscd, Cdscb are extracted. The parameter C_{it} in Eq. (2.7.3) is the capacitance due to interface states. From Eq. (2.7.3), it can be seen that subthreshold swing shares the same exponential dependence on channel length as the *DIBL* effect. The parameter *Nfactor* is introduced to compensate for errors in the depletion width capacitance calculation. *Nfactor* is determined experimentally and is usually very close to 1.

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2.8 Effective Channel Length and Width:

The effective channel length and width used in all model expressions is given below:

$$L_{eff} = L_{drawn} - 2dL \tag{2.8.1}$$

$$W_{eff} = W_{drawn} - 2dW \tag{2.8.2a}$$

$$W_{eff}' = W_{drawn} - 2dW' \tag{2.8.2b}$$

The only difference between Eq. (2.8.1a) and (2.8.1b) is that the former includes bias dependencies. The parameters dW and dL are modeled by the following:

$$dW = dW' + dW_g V_{gsteff} + dW_b (\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}) \tag{2.8.3}$$

$$dW' = W_{\text{int}} + \frac{W_l}{L^{W\ln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{W\ln} W^{Wwn}}$$

$$dL = L_{\text{int}} + \frac{L_l}{L^{L\ln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{L\ln} W^{Lwn}} \tag{2.8.4}$$

These complicated formulations require some explanation. From Eq. (2.8.3), the variable W_{int} models represents the tradition manner from which "delta W" is extracted (from the *int*ercepts of straights lines on a $1/R_{ds}$ vs. W_{drawn} plot). The parameters dW_g and dW_b have been added to account for the contribution of both front gate and back side (substrate) biasing effects. For *dL*, the parameter L_{int}

represents the traditional manner from which "delta L" is extracted (mainly from the *int*ercepts of lines from a R_{ds} vs. L_{drawn} plot).

The remaining terms in both *dW* and *dL* are included for the convenience of the user. They are meant to allow the user to model each parameter as a function of W(drawn), L(drawn), and their associated product terms. In addition, the freedom to model these dependencies as other than just simple inverse functions of W and L is also provide for the user in BSIM3v3. For *dW*, they are *Wln* and *Wwn*. For *dL* they are *Lln* and *Lwn*.

By default all of the above *geometrical* dependencies for both dW and dL are turned off. Again, these equations are provided in BSIM3v3 only for the convenience of the user. As such, it is up to the user must adopt the correct extraction strategy to ensure proper use.

2.9 Poly Gate Depletion Effect

When a gate voltage is applied to a heavily doped poly-silicon gate, e.g. NMOS with n+ poly-silicon gate, a thin depletion layer will be formed at the interface between the poly-silicon and gate oxide. Although this depletion layer is very thin due to the high doping concentration of the poly-Si gate, its effect cannot be ignored in the 0.1µm regime since the gate oxide thickness will also be very small, possibly 50Å or thinner.

Figure 2-7 shows a NMOSFET with a depletion region in the n+ poly-silicon gate. The doping concentration in the n+ poly-silicon gate is N_{gate} and the doping concentration in the substrate is N_{sub}. The gate oxide thickness is T_{ox}. The depletion width in the poly gate is X_p. The depletion width in the substrate is X_d. If we

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assume the doping concentration in the gate is infinite, then no depletion region will exist in the gate, and there would be one sheet of positive charge whose thickness is zero at the interface between the poly-silicon gate and gate oxide.

In reality, the doping concentration is, of course, finite. The positive charge near the interface of the poly-silicon gate and the gate oxide is distributed over a finite depletion region with thickness X_p. In the presence of the depletion region, the voltage drop across the gate oxide and the substrate will be reduced, because part of the gate voltage will be dropped across the depletion region in the gate. That means the effective gate voltage will be reduced.

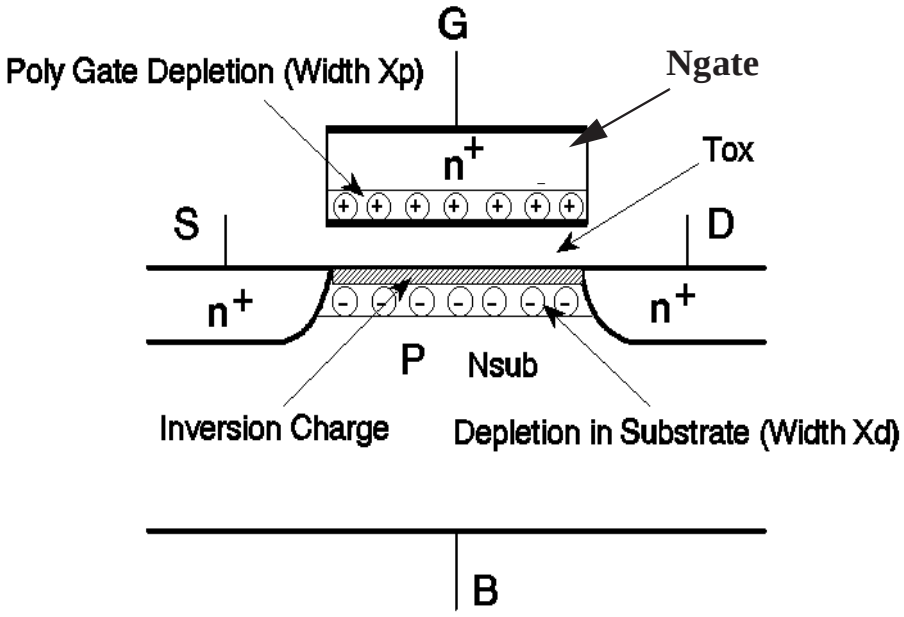

Figure 2-7. Charge distribution in a MOSFET with the poly gate depletion effect. The device is in the strong inversion region.

The effective gate voltage can be calculated in the following manner. Assume the doping concentration in the poly gate is uniform. The voltage drop in the poly gate (V_{poly}) can be calculated as:

$$V_{poly} = \frac{1}{2} X_{poly} E_{poly} = \frac{qN_{gate} X_{poly}^2}{2\varepsilon_{si}} \tag{2.9.1}$$

where E_{poly} is the maximum electrical field in the poly gate. The boundary condition at the interface of poly gate and the gate oxide is

$$\varepsilon_{ox} E_{ox} = \varepsilon_{si} E_{poly} = \sqrt{2q\varepsilon_{si} N_{gate} V_{poly}} \tag{2.9.2}$$

where E_{ox} is the electrical field in the gate oxide. The gate voltage satisfies

$$V_{gs} - V_{FB} - \phi_s = V_{poly} + V_{ox} \tag{2.9.3}$$

where V_{ox} is the voltage drop across the gate oxide and satisfies $V_{ox} = E_{ox}T_{ox}$.

According to the equations (2.9.1) to (2.9.3), we obtain the following:

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0 \tag{2.9.4}$$

where (2.9.5)

$$a = \frac{\varepsilon_{ox}^2}{2q\varepsilon_{si} N_{gate} T_{ox}^2}$$

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By solving the equation (2.9.4), we get the effective gate voltage (V_{gs_eff}) which is equal to:

$$V_{gs\_eff} = V_{FB} + \phi_s + \frac{q\varepsilon_{si}N_{gate}T_{ox}^2}{\varepsilon_{ox}^2}\left(\sqrt{1+\frac{2\varepsilon_{ox}^2(V_{gs}-V_{FB}-\phi_s)}{q\varepsilon_{si}N_{gate}T_{ox}^2}}-1\right) \quad (2.9.6)$$

Figure 2-8 shows V_{gs_eff} / V_{gs} versus the gate voltage. The threshold voltage is assumed to be *0.4V*. If T_{ox} = *40 Å*, the effective gate voltage can be reduced by *6%* due to the poly gate depletion effect as the applied gate voltage is equal to *3.5V*.

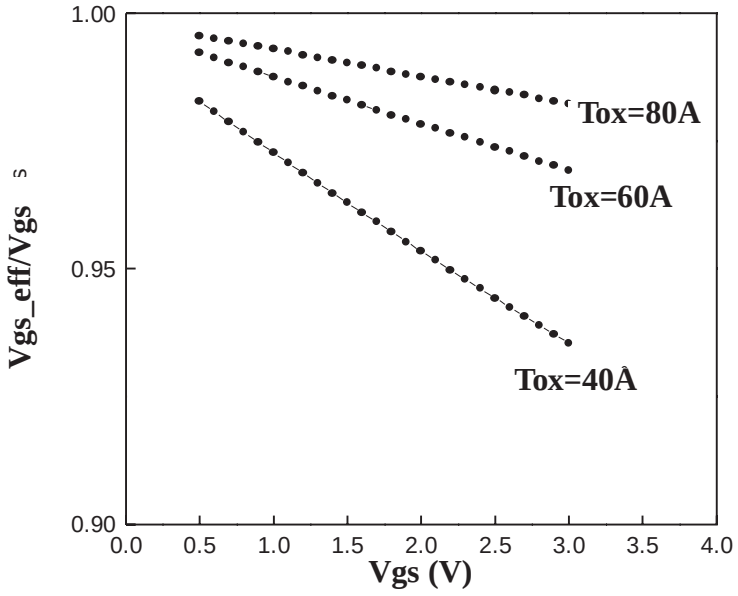

Figure 2-8. The effective gate voltage versus applied gate voltage at different gate oxide thickness.

The drain current reduction in the linear region as a function of the gate voltage can now be determined. Assume the drain voltage is very small, e.g. *50mV*. Then

the linear drain current is proportional to $C_{ox}(V_{gs} - V_{th})$. The ratio of the linear drain current with and without poly gate depletion is equal to:

$$\frac{I_{ds}(V_{gs\_eff})}{I_{ds}(V_{gs})} = \frac{(V_{gs\_eff} - V_{th})}{(V_{gs} - V_{th})} \tag{2.9.7}$$

Figure 2-9 shows Ids(Vgs_eff) / Ids(Vgs) versus the gate voltage using eq. (2.9.7). The drain current can be reduced by several percent due to gate depletion.

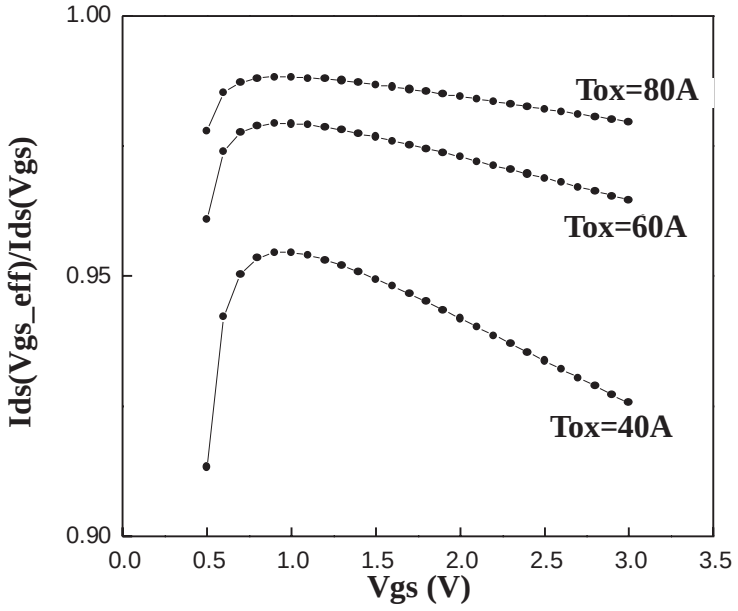

Figure 2-9. Ratio of linear region current with poly gate depletion effect and that without.

CHAPTER 3: Unified I-V Model

The development of separate model expressions for such device operation regimes as subthreshold and strong inversion were discussed in Chapter 2. Although these expressions can each accurately describe device behavior within their own respective region of operation, problems are likely to occur between two well-described regions or within transition regions. In order to circumvent this issue, a unified model should be synthesized to not only preserve region-specific expressions but also to ensure the continuities of current (Ids) and conductance (G_X) *and* their derivatives in *all* transition regions as well. Such high standards are met in BSIM3v3. As a result, convergence and calculation efficiencies are much improved.

This chapter will describe the unified natured of BSIM3v3's model equations. While most of the parameter symbols in this chapter are explained in the following text, a complete description of all I-V model equation parameters can be found in the Appendix A.

3.1 Unified Channel Charge Density Expression

Separate expressions for channel charge density are shown below for subthreshold (Eq. (3.1.1a) and (3.1.1b)) and strong inversion (Eq. (3.1.2)). Both expressions are valid for small Vds.

(3.1.1a)

$$Q_{chsubs0} = Q_0 \exp(\frac{V_{gs} - V_{th}}{n v_t})$$

where, Q_0 is:

(3.1.1b)

$$Q_0 = \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}} v_t \exp(-\frac{V_{off}}{n v_t})$$

(3.1.2)

$$Q_{chs0} = C_{ox}(V_{gs} - V_{th})$$

In both Eqs. (3.1.1a) and (3.1.2), the parameters $Q_{chsubs0}$ and Q_{chs0} are the channel charge densities at the source for very small Vds. To form a unified expression, an effective (Vgs-Vth) function named Vgsteff is introduced to describe the channel charge characteristics from subthreshold to strong inversion:

(3.1.3)

$$V_{gsteff} = \frac{2\, n\, v_t \ln\left[1 + \exp(\frac{V_{gs} - V_{th}}{2\, n\, v_t})\right]}{1 + 2\, n\ \ C_{OX}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si}N_{ch}}} \exp(-\frac{V_{gs} - V_{th} - 2V_{off}}{2\, n\, v_t})}$$

The unified channel charge density at the source end for both subthreshold and inversion region can therefore be written as:

(3.1.4)

$$Q_{chs0} = C_{ox} V_{gsteff}$$

Figures 3-1 and 3-2 show the "smoothness" of Eq. (3.1.4) from subthreshold to strong inversion regions. The Vgsteff expression will be used again in subsequent sections of this chapter to model the drain current.

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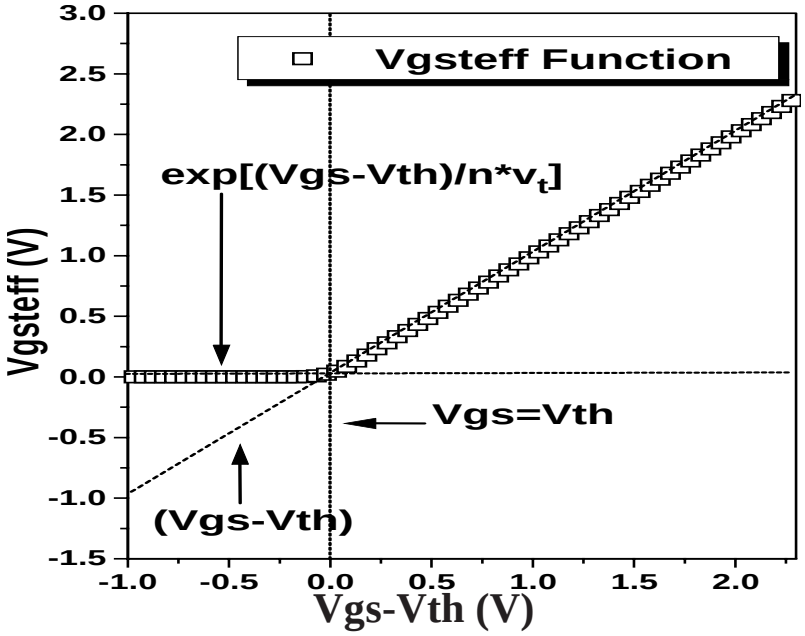

Figure 3-1. The Vgsteff function vs. (Vgs-Vth) in linear scale.

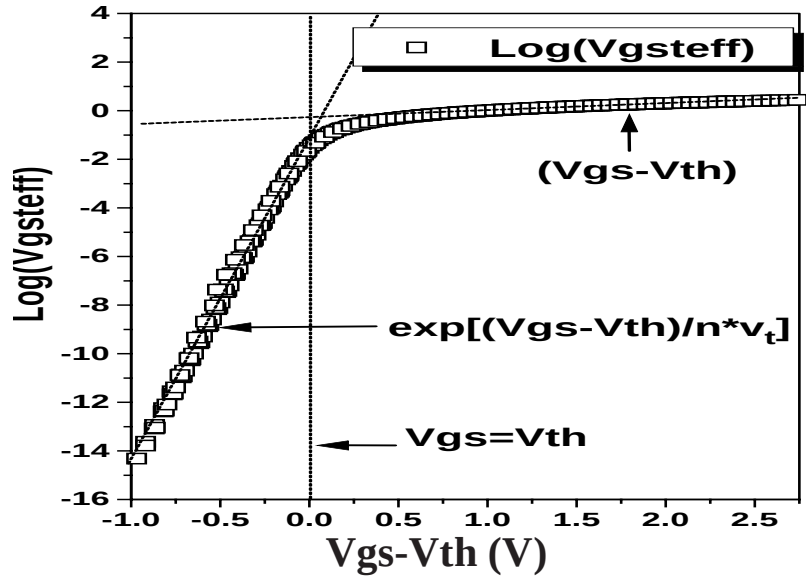

Figure 3-2. Vgsteff function vs. (Vgs-Vth) in log scale.

Eq. (3.1.4) serves as the cornerstone of the unified channel charge expression at the source for small Vds. To account for the influence of Vds, the Vgsteff function must keep track of the change in channel potential from the source to the drain. In other words, Eq. (3.1.4) will have to include a y dependence. To initiate this formulation, consider first the re-formulation of channel charge density for the case of **strong inversion:**

$$Q_{chs(y)} = C_{ox}(V_{gs} - V_{th} - A_{bulk}V_{F(y)}) \tag{3.1.5}$$

The parameter $V_{F(y)}$ stands for the quasi-Fermi potential at any given point, y, along the channel with respect to the source. This equation can also be written as:

$$Q_{chs(y)} = Q_{chs0} + \Delta Q_{chs(y)} \tag{3.1.6}$$

The term $\Delta Q_{chs(y)}$ is the incremental channel charge density induced by the drain voltage at point y. It can be expressed as:

$$\Delta Q_{chs(y)} = -CoxA_{bulk}V_{F(y)} \tag{3.1.7}$$

For the **subthreshold region** (Vgs<<Vth), the channel charge density along the channel from source to drain can be written as:

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$$Q_{chsubs(y)} = Q_0 \exp(\frac{V_{gs} - V_{th} - A_{bulk}V_{F(y)}}{nv_t}) \quad (3.1.8)$$
$$= Q_{chsubs0} \exp(-\frac{A_{bulk}V_{F(y)}}{nv_t})$$

A Taylor series expansion of the right-hand side of Eq. (3.1.8) yields the following (keeping only the first two terms):

$$Q_{chsubs(y)} = Q_{chsubs0}(1 - \frac{A_{bulk}V_{F(y)}}{nv_t}) \quad (3.1.9)$$

Analogous to Eq. (3.1.6), Eq. (3.1.9) can also be written as:

$$Q_{chsubs(y)} = Q_{chsubs0} + \Delta Q_{chsubs(y)} \quad (3.1.10)$$

The parameter $\Delta Q_{chsubs(y)}$ is the incremental channel charge density induced by the drain voltage in the subthreshold region. It can be written as:

$$\Delta Q_{chsubs(y)} = -\frac{A_{bulk}V_{F(y)}}{nv_t} Q_{chsubs0} \quad (3.1.11)$$

Note that Eq. (3.1.9) is valid only when $V_{F(y)}$ is very small, which is maintained, fortunately, due to the fact that Eq. (3.1.9) is only used in the linear regime (i.e. Vds ≤2vt).

Eqs. (3.1.6) and (3.1.10) both have drain voltage dependencies. However, they are decuple and a unified expression for $Q_{ch(y)}$ is desperately needed. To obtain a unified expression along the channel, we first assume:

$$\Delta Q_{ch(y)} = \frac{\Delta Q_{chs(y)} \Delta Q_{chsubs(y)}}{\Delta Q_{chs(y)} + \Delta Q_{chsubs(y)}} \tag{3.1.12}$$

Here, $\Delta Q_{ch(y)}$ is the incremental channel charge density induced by the drain voltage. Substituting Eq. (3.1.7) and (3.1.11) into Eq. (3.1.12), we obtain:

$$\Delta Q_{ch(y)} = \frac{V_{F(y)}}{Vb} Q_{chs0} \tag{3.1.13}$$

where V_b=*(Vgsteff+n*v$_t$)/A$_{bulk}$*. In order to remove any association between the variable *n* and bias dependencies (Vgsteff) as well as to ensure more precise modeling of Eq. (3.1.8) for linear regimes (under subthreshold conditions), the variable *n* is replaced with 2. The expression for V_b now becomes:

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}} \tag{3.1.14}$$

A unified expression for $Q_{ch(y)}$ from subthreshold to strong inversion regimes is now at hand:

$$Q_{ch(y)} = Q_{chs0}\left(1 - \frac{V_{F(y)}}{V_b}\right) \tag{3.1.15}$$

The variable Q_{chs0} is given by Eq. (3.1.4).

3.2 Unified Mobility Expression

BSIM3v3 uses a unified mobility expression based on the Vgsteff expression of Eq. 3.1.3. Thus, we have:

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(Mobmod=1) (3.2.1)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2}$$

To account for depletion mode devices, another mobility model option is given by the following:

(Mobmod=2) (3.2.2)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_{a\,+} U_c V_{bseff})(\frac{V_{gsteff}}{T_{OX}}) + U_b(\frac{V_{gsteff}}{T_{OX}})^2}$$

To consider the body bias dependence of Eq. 3.2.1 further, we have introduced the following expression:

(For Mobmod=3) (3.2.3)

$$\mu_{eff} = \frac{\mu_o}{1 + [U_a(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2](1 + U_c V_{bseff})}$$

3.3 Unified Linear Current Expression

3.3.1 Intrinsic case (Rds=0)

Generally, the following expression [2] is used to account for both drift and diffusion current:

$$I_{d(y)} = WQ_{ch(y)}\mu_{ne(y)}\frac{dV_{F(y)}}{dy} \tag{3.3.1}$$

where the parameter $u_{ne(y)}$ can be written as:

$$\mu_{ne(y)} = \frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}} \tag{3.3.2}$$

Substituting Eq. (3.3.2) in Eq. (3.3.1) we get:

$$I_{d(y)} = WQ_{chso}(1-\frac{V_{F(y)}}{V_b})\frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}}\frac{dV_{F(y)}}{dy} \tag{3.3.3}$$

Eq. (3.3.3) resembles the equation used to model drain current in the strong inversion regime. However, it can now be used to describe the current characteristics in the subthreshold regime when Vds is very small (Vds<$2v_t$). Eq. (3.3.3) can now be integrated from the source to drain to get the expression for linear drain current in the channel. This expression is valid from the subthreshold regime to the strong inversion regime:

$$I_{ds0} = \frac{W\mu_{eff}Q_{chs0}V_{ds}(1-\frac{V_{ds}}{2V_b})}{L(1+\frac{V_{ds}}{V_a})} \tag{3.3.4}$$

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3.3.2 Extrinsic Case (Rds > 0)

The current expression when Rds > 0 can be obtained based on Eq. (2.5.9) and Eq. (3.3.4). The expression for linear drain current from subthreshold to strong inversion is:

$$I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds} I_{dso}}{V_{ds}}} \tag{3.3.5}$$

Chapter 8 will illustrate the "smoothness" of this expression.

3.4 Unified Vdsat Expression

3.4.1 Intrinsic case (Rds=0)

To get an expression for the electric field as a function of y along the channel, we integrate Eq. (3.3.1) from 0 to an arbitrary point y. The expression is as follows:

$$E_y = \frac{I_{dso}}{\sqrt{(WQ_{chs0}\mu_{eff} - \frac{I_{dso}}{E_{sat}})^2 - \frac{2 I_{ds0} W Q_{chs0} \mu_{eff} y}{V_b}}} \tag{3.4.1}$$

If we assume that drift velocity saturates when *Ey=Esat*, we get the following expression for Idsat:

(3.4.2)

$$I_{dsat} = \frac{W\mu_{eff}Q_{chs0}E_{sat}LV_b}{2L(E_{sat}L + V_b)}$$

Let *Vds=Vdsat* in Eq. (3.3.4) and set this equal to Eq. (3.4.2), we get the following expression for *Vdsat*:

(3.4.3)

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2\nu_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2\nu_t}$$

3.4.2 Extrinsic Case (Rds>0)

The Vdsat expression for the extrinsic case is formulated from Eq. (3.4.3) and Eq. (2.5.10) to be the following:

(3.4.4a)

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

where,

(3.4.4b)

$$a = A_{bulk}{}^2W_{eff}\nu_{sat}C_{ox}R_{DS} + (\frac{1}{\lambda} - 1)A_{bulk}$$

(3.4.4c)

$$b = -\left((V_{gsteff} + 2\nu_t)(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}(V_{gsteff} + 2\nu_t)W_{eff}\nu_{sat}C_{ox}R_{DS}\right)$$

(3.4.4d)

$$c = (V_{gsteff} + 2\nu_t)E_{sat}L_{eff} + 2(V_{gsteff} + 2\nu_t)^2W_{eff}\nu_{sat}C_{ox}R_{DS}$$

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(3.4.4e)

$$\lambda = A_1 V_{gsteff} + A_2$$

The parameter λ is introduced to account for non-saturation effects. The parameters A_1 and A_2 are extracted.

3.5 Unified Saturation Current Expression

A unified expression for the saturation current from the subthreshold to the strong inversion regime can be formulated by introducing the Vgsteff function into Eq. (2.6.15). The resulting equations are the following:

(3.5.1)

$$I_{ds} = \frac{I_{dso(Vdsat)}}{1 + \frac{R_{ds} I_{dso(Vdsat)}}{V_{dsat}}} \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}}\right)$$

where,

(3.5.2)

$$V_A = V_{Asat} + (1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1}$$

(3.5.3)

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2 R_{DS} \nu_{sat} C_{ox} W_{eff} V_{gsteff} [1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2\nu_t)}]}{2 / \lambda - 1 + R_{DS} \nu_{sat} C_{ox} W_{eff} A_{bulk}}$$

(3.5.4)

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat}\, litl} (V_{ds} - V_{dsat})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout} t(1 + P_{DIBLCB} V_{bseff})}\left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t}\right) \tag{3.5.5}$$

$$\theta_{rout} = P_{DIBLC1}\left[\exp(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}) + 2\exp(-D_{ROUT}\frac{L_{eff}}{l_{t0}})\right] + P_{DIBLC2} \tag{3.5.6}$$

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}\, litl}{V_{ds} - V_{dsat}}\right) \tag{3.5.7}$$

3.6 Single Current Expression for All Operational Regimes of Vgs and Vds

The Vgsteff function introduced in Chapter 2 gave a unified expression for the linear drain current from subthreshold to strong inversion as well as for the saturation drain current from subthreshold to strong inversion, *separately.* In order to link the continuous linear current with that of the continuous saturation current, a smooth function for Vds is introduced. In the past, several smooth functions have been proposed for MOSFET modeling [22-24]. For BSIM3v3, the smooth function used is similar to that proposed by R. M. D. A. Velghe et al [24]. The overall current equation for both linear and saturation current now becomes:

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \tag{3.6.1}$$

Most of the previous equations which contain *Vds* and *Vdsat* dependencies are now substituted with the *Vdseff* function. For example, Eq. (3.5.4) now becomes:

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(3.6.2)

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\ litl}(V_{ds} - V_{dseff})$$

Similarly, Eq. (3.5.7) now becomes:

(3.6.3)

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}\ litl}{V_{ds} - V_{dseff}}\right)$$

The Vdseff expression is written as:

(3.6.4)

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

The expression for Vdsat is that given under Section 3.4. The parameter δ is an extracted constant. The dependence of Vdseff on Vds is given in Figure 3-3. The Vdseff function follows Vds in the linear region and tends to Vdsat in the saturation region. Figure 3-4 shows the effect of δ on the transition region between linear and saturation regimes.

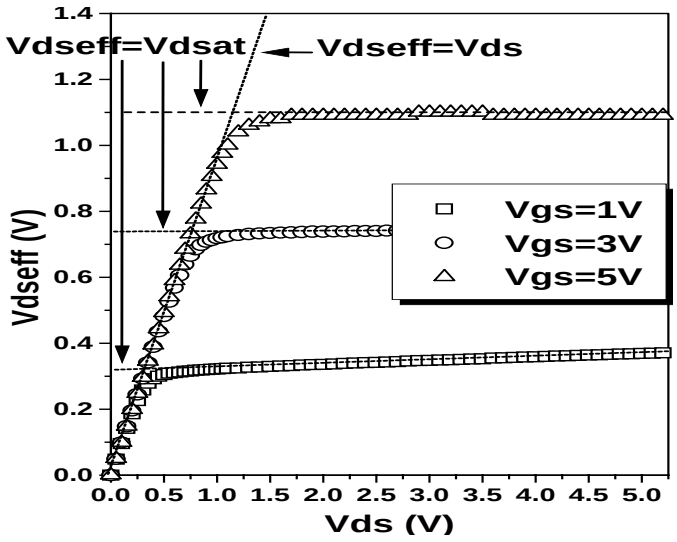

Figure 3-3. Vdseff vs. Vds for δ=0.01 and different Vgs.

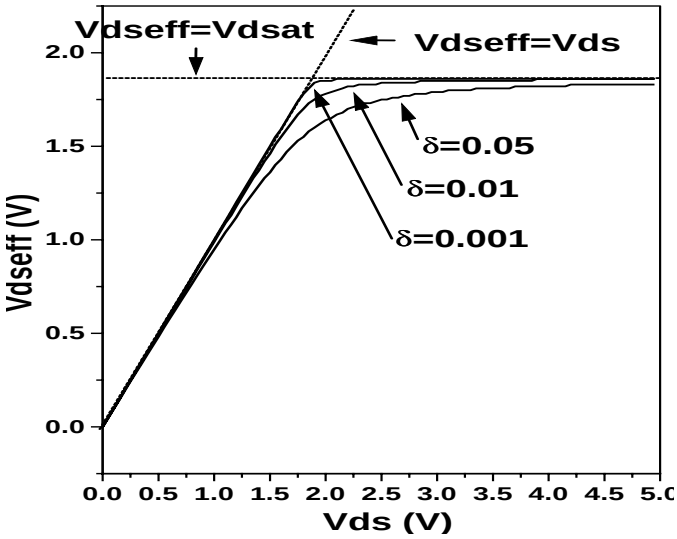

Figure 3-4. Vdseff vs. Vds for Vgs=3V and different δ values.

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3.7 Substrate Current

BSIMv3 uses the Eq. (3.7.1) to model substrate current.

$$I_{sub} = \frac{\alpha_o}{L_{eff}}(V_{ds} - V_{dseff}) \exp(-\frac{\beta_o}{V_{ds} - V_{dseff}}) \frac{I_{dso}}{1 + \frac{R_{ds} I_{dso}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right) \tag{3.7.1}$$

The parameters $\alpha 0$ and $\beta 0$ refer to impact ionization current.

3.8 A Note on Vbs

In BSIM3v3, all Vbs terms which have appeared in Chapters 2 and 3 have been substituted with a Vbseff expression as shown in Eq. (3.8.1). This is done in order to set an upper bound for the body bias value during simulations. Unreasonable values can occur if this expression is not introduced.

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\ ] \tag{3.8.1}$$

where δ_1=0.001.

The parameter *Vbc* is the maximum allowable V_{bs} value and is obtained based on the condition of dV_{th}/dV_{bs}=0 for the V_{th} expression of 2.1.4.

CHAPTER 4: Capacitance Model

Previous BSIM capacitance models used long channel charge models in which the ratio of C_{ij}/L_{eff} (where i and j are the transistor nodes) did not scale with L_{eff}. This resulted in an overestimation of capacitance values for devices smaller than a L_{drawn} of 2 μm. This effect was particularly severe at low drain biases. In addition, previous capacitance models also showed appalling discontinuities for the gate capacitance at threshold voltage. These factors as wells as others necessitated the development of a new charge and capacitance model.

4.1 General Information

In BSIM3v3, a new capacitance formulation addresses the above concerns. This new model incorporates the following enhancements:

- Separate effective channel length and width are used for capacitance and I-V models.
- A simple short channel capacitance model with accuracy down to the 0.2 μm Leff range.
- Intrinsic C-V model is no longer piece-wise (i.e. divided into inversion, depletion, triode and saturation regions). Instead, a single equation is used for each nodal charge covering all regions of operation. This ensures continuity of all derivatives and enhances convergence properties. The inversion

capacitance and substrate capacitance are also no longer discontinuous at the threshold voltage.

- Threshold voltage formulation is consistent with the I-V model. Effects such as body effect and DIBL are automatically incorporated in the capacitance model.
- Overlap capacitance comprises two parts: 1) a bias independent part which models the effective overlap capacitance between the gate and the heavily doped source/drain, and 2) a gate bias dependent part between the gate and the lightly doped source/drain region.
- Bias independent, fringing capacitances are added between the gate and source as well as the gate and drain.

To accommodate these changes, new parameters are introduced (Table 4-1).

Name	Function	Default	Unit
CAPMOD	Flag for short channel capacitance model	2	(True)
CGS1	Lightly-doped source to gate overlap capacitance	0	(F/m)
CGD1	Lightly-doped drain to gate overlap capacitance	0	(F/m)
CKAPPA	Coefficient for lightly-doped overlap capacitance	0.6	
CF	Fringing field capacitance	equation (4.4.2)	(F/m)
CLC	Constant term for short channel model	0.1	μm
CLE	Exponential term for short channel model	0.6	
DWC	Long channel gate capacitance width offset	Wint	μm
DLC	Long channel gate capacitance length offset	Lint	μm

Table 4-1. New parameters for BSIM3v3 capacitance model.

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4.2 A Note on Device Geometry Dependencies

For capacitance modeling considerations, a transistor can be divided into 2 regions: intrinsic and extrinsic. The **intrinsic** part is the region between the metallurgical source and drain junction when the gate to S/D region is at flat band voltage. The **extrinsic** part, basically the parasitics, is further divided into three regions: 1) the outer fringing capacitance between the polysilicon gate and the source/drain, 2) the overlap between the gate and the heavily doped S/D region (relatively insensitive to bias conditions), and 3) the overlap between the gate and lightly doped S/D region which changes with bias.

In the previous C-V model (BSIM3 Version 2.0), both the I-V and C-V parts of the model used the same Leff and Weff expressions.. This is not so in the new model BSIM3v3. The geometry dependence for the **intrinsic** capacitance part is given as the following:

$$\delta W_{eff} = DWC + \frac{Wl}{L^{\mathrm{Wln}}} + \frac{Ww}{W^{Wwn}} + \frac{Wwl}{L^{Wln} W^{Wwn}} \tag{4.2.1}$$

$$\delta L_{eff} = DLC + \frac{Ll}{L^{Lln}} + \frac{Lw}{W^{Lwn}} + \frac{Lwl}{L^{Lln} W^{Lwn}} \tag{4.2.2}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff} \tag{4.2.3}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff} \tag{4.2.4}$$

The meanings of *DWC* and *DLC* are different from those of *Wint* and *Lint* in the I-V model. L_{active} and W_{active} are the effective length and width of the intrinsic

device for capacitance calculations. Unlike the case with I-V, we assumed that these dimensions have no voltage bias dependence. The parameter δLeff is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate printing, etching and oxidation) on one side. Overall, a distinction should be made between the effective channel length extracted from the capacitance measurement and from the I-V measurement.

Traditionally, the Leff extracted during I-V model characterization is used to gauge a technology. However this Leff does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation so that the measured I-V characteristics match those calculated by the model. This Leff is therefore very sensitive to the I-V equations used and also to the conduction characteristics of the LDD region relative to the channel region. A device with a large Leff and a small parasitic resistance can have a similar current drive as another with a smaller Leff but larger R_{ds}. In some cases Leff can be larger than the polysilicon gate length giving Leff a dubious physical meaning (negative Leff).

The L_{active} parameter extracted from the capacitance method is a closer representation of the metallurgical junction length (physical length). Due to the graded source/ drain junction profile the source to drain length can have a very strong bias dependence. We therefore define L_{active} to be that measured at gate to source/drain flat band voltage. If the values for *DWC* and *DLC* are not specified in the SPICE model card, BSIM3v3's capacitance model will assume that the device in question has the same effective dimensions for both I-V and C-V models (i.e. *DWC = Wint* and *DLC=Lint).*

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4.3 Intrinsic Capacitance

4.3.1 Background Information

There has been no recent major work performed in the area of intrinsic capacitance modeling suitable for implementation into a circuit simulator. One bottleneck is the difficulty in capacitance measurement, especially in the deep micron regime. At very short channel lengths, the MOSFET intrinsic capacitance is very small yet the conductance is large. The large conductance results in large in-phase currents during high frequency measurement and overloads the C-V meter. Also the effects of the parasitic inductance in the experimental setup will be more profound. Moreover, since charge can only be measured at high impedance nodes (i.e. the gate and substrate nodes), only 8 of the 16 capacitance components in an intrinsic MOSFET, can be directly measured.

An alternative solution is to use a 2-D device simulator such as PISCES. However, the simulation results are not always satisfactory. Another reason for the lack of development work is the observation that most circuits used to be dominated by interconnect and junction capacitances. An exact model for the intrinsic transistor capacitance is of lesser importance. However, this may no longer be true with the continuous shrinking of design rules. Also, a well behave capacitance model will help circuit simulation convergence. In low power and analog applications, designers are interested in device operation near threshold voltage. Thus, the model must also be accurate in transition regions as well. To ensure proper behavior, both the I-V and C-V model equations should be

developed from an identical set of charge equations so that C_{ij}/I_d is well behaved.

Similar to the I-V model, the development of the capacitance model was carried out with an effort to balance physics with simulation efficiency. Several physical models have been published. These were either too complicated or lacked continuity from one operation region to another. A good model should be simple yet include most of the physical concepts.

4.3.2 Basic Formulation

To ensure charge conservation, terminal charges instead of the terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain, respectively. The gate charge is comprised of mirror charges from 3 components: the channel minority (inversion) charge (Q_{inv}), the channel majority (accumulation) charge (Q_{acc}) and the substrate fix charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate node while the channel charge comes from the source and drain nodes:

(4.3.1)

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases}$$

The substrate charge can be divided into two components - the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to

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substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (δQ_{sub}). Q_g now becomes:

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub}\right) \tag{4.3.2}$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by:

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y \tag{4.3.3}$$

(4.3.4)

$$\text{therefore} \quad \begin{cases} Q_c = W_{active} \int_0^{L_{active}} q_c dy = W_{active} C_{ox} \int_0^{L_{active}} \left(V_{gt} - A_{bulk} V_y\right) dy \\ Q_g = W_{active} \int_0^{L_{active}} q_g dy = W_{active} C_{ox} \int_0^{L_{active}} \left(V_{gt} + V_{th} - V_{FB} - \phi_s - V_y\right) dy \\ Q_b = W_{active} \int_0^{L_{active}} q_b dy = -W_{active} C_{ox} \int_0^{L_{active}} \left(V_{th} - V_{FB} - \phi_s - (1 - A_{bulk}) V_y\right) dy \end{cases}$$

Substituting the following:

$$dy = \frac{dV_y}{\varepsilon_y}$$

and

$$J_{ds} = \frac{\mu_{eff} C_{ox}}{L_{active}} \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds}\right) V_{ds} = \mu_{eff} C_{ox} \left(V_{gt} - A_{bulk} V_{ds}\right) \varepsilon_y \tag{4.3.5}$$

into Eq. (4.3.4), we have the following upon integration:

(4.3.6)

$$\begin{cases} Q_c = -W_{active} L_{active} C_{ox} \left(\left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right) + \frac{A_{bulk}^{\ 2} V_{ds}^{\ 2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \\ Q_b = -Q_g - Q_c = Q_{sub0} + \delta Q_{sub} \\ Q_g = -Q_{sub0} + W_{active} L_{active} C_{ox} \left(\left(V_{gt} - \frac{V_{ds}}{2} \right) + \frac{A_{bulk} V_{ds}^{\ 2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \end{cases}$$

where,

(4.3.7)

$$\begin{cases} Q_{sub0} = -W_{active} L_{active} \sqrt{2 \varepsilon_{Si} q N_b \left(2 \phi_b - V_{bs} \right)} \\ \delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}}{2} V_{ds} - \frac{\left(1 - A_{bulk} \right) A_{bulk} V_{ds}^{\ 2}}{12 \left(V_{active} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \end{cases}$$

The inversion charges are supplied from the source and drain electrodes such that $Q_{inv} = Q_s + Q_d$. The ratio of Q_d and Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 0, 0.5 and 1) which are the ratios of Q_d to Q_s in the saturation region. We will revisit charge partitioning in Section 4.3.4.

All capacitances are derived from the charges to ensure charge conservation. Since there are 4 nodes, there are altogether 16 components. For each component:

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(4.3.8)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where i and j denote transistor nodes. In addition:

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

4.3.3 Short Channel Model

In deriving the long channel charge model, mobility is assumed to be constant with no velocity saturation. Therefore in the saturation region ($V_{ds} \geq V_{dsat}$), the carrier density at the drain end is zero. Since no channel length modulation is assumed, the channel charge will remain a constant throughout the saturation region. In essence, the channel charge in the saturation region is assumed to be zero. This is a good approximation for long channel devices but fails when $L_{eff} < 2$ μm. If we define a drain bias, $V_{dsat,cv}$, in which the channel charge becomes a constant, we will find that $V_{dsat,cv}$ in general is larger than V_{dsat} but smaller than the long channel V_{dsat}, given by V_{gt}/A_{bulk} (A_{bulk} is a parameter modeling the non-uniform substrate charge). However, in the old long channel charge model $V_{dsat,cv}$ is set to V_{gt}/A_{bulk} independent of channel length. Consequently, C_{ij}/Leff also has no channel length dependence (Eqs. (4.3.6), (4.37)). A pseudo short channel modification from the long channel has been used in the past. It involved the parameter A_{bulk} in the capacitance model which was redefined to be equal to V_{gt}/V_{dsat}, thereby equating $V_{dsat,cv}$ and V_{dsat}. This

overestimated the effect of velocity saturation and resulted in a smaller channel capacitance.

The difficulty in developing a short channel model lies in calculating the charge in the saturation region. Although current continuity stipulates that the charge density in the saturation region is almost constant, it is difficult to calculate accurately the length of the saturation region. Moreover, due to the exponentially increasing lateral electric field, most of the charge in the saturation region are not controlled by the gate electrode. However, one would expect that the total charge in the channel will exponentially decrease with drain bias. A physical model has been developed to reflect this but will not be presented here. A simpler model is adopted to empirically fit $V_{dsat,cv}$ to channel length. Experimentally,

(4.3.9)

$$V_{dsat,iv} < V_{dsat,cv} < V_{dsat,iv}\Big|_{L_{active}\to\infty} = \frac{V_{gsteff,cv}}{A_{bulk}}$$

and Vdsat,cv is fitted empirically by the following:

(4.3.10a)

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right)}$$

(4.3.10b)

$$V_{gsteff,cv} = nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}}{nv_t}\right)\right)$$

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The parameter A_{bulk} can now be substituted by A_{bulk}' in the long channel equation where:

$$A_{bulk}' = A_{bulk0}\left(1+\left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right) \tag{4.3.11}$$

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_o}{W_{eff}'+B_1}\right\}\right)\frac{1}{1+K_{ETA}V_{bseff}} \tag{4.3.11a}$$

By setting *CLC* to zero, the new model reduces back to the old model. At very short channel lengths where velocity overshoot is prominent, the channel charges is only a weak function of channel length and saturation velocity. The effect of velocity overshoot is minimal and is not implemented into the model.

4.3.4 New Single Equation Formulation

In the old formulation, the capacitance is divided into four regions. There were separate equations modeling the nodal charges in each region. From one region to another the charges were conserved, but not their slopes. Therefore, the capacitances in some of these transitions were discontinuous. In the new model, a single equation is used to model each charge for all regions.

(a) Transition from depletion to inversion region

The biggest discontinuity is the inversion capacitance at threshold voltage. The old model uses a step function and the inversion capacitance changes

abruptly from 0 to C_{ox}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to 0 at threshold voltage. Both of these effects cause oscillation during circuit simulation. Experimentally, capacitance starts to increase almost quadratically at ~0.2V below threshold voltage and levels off at ~0.3V above threshold voltage. For analog and low power circuits, an accurate capacitance model around the threshold voltage is very important.

The non-abrupt channel inversion capacitance and substrate capacitance model is developed from the new I-V model which uses a single equation to formulate the subthreshold, transition and inversion regions. The new channel inversion charge model can be modified to any charge model by substituting V_{gt} with $V_{gsteff,cv}$ as in the following:

$$Q_{(inv,s,d)}(V_{gt}) = Q_{(inv,s,d)}(V_{gsteff,cv}) \tag{4.3.12}$$

Now,

$$\begin{cases} C_{(inv,s,d),g}(V_{gt}) = C_{(inv,s,d),g}(V_{gsteff,cv})\dfrac{\partial V_{gxt}}{\partial V_{gs}} \\ C_{(inv,s,d),(s,d,b)}(V_{gt}) = C_{(inv,s,d),(s,d,b)}(V_{gsteff,cv}) \end{cases} \tag{4.3.13}$$

where,

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(4.3.14)

$$\frac{\partial V_{gsteff,cv}}{\partial V_{gs}} = \frac{\exp\left(\frac{V_{gst}}{nv_t}\right)}{\left(1 + \exp\left(\frac{V_{gst}}{nv_t}\right)\right)}$$

The "inversion" (minority) charge is always non-zero, even in the accumulation region. However, it decreases exponentially with gate bias in the subthreshold region.

(b) Transition from accumulation to depletion region

A parameter VFBeff is used to smooth out the transition between accumulation and depletion regions. It affects the accumulation and depletion charges:

(4.3.16)

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3^{\,2} + 4\delta_3 vfb}\right\} \quad where \quad V_3 = vfb - V_{gb} - \delta_3; \quad \delta_3 = 0.02$$

(4.3.16a)

$$vfb = V_{th} - \phi_s - K_1\sqrt{\phi_s}$$

(4.3.17)

$$Q_{acc} = -W_{active} L_{active} C_{ox} \left(V_{FBeff} - vfb\right)$$

(4.3.18)

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1^{\,2}}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FBeff} - V_{gsteff\,cv} - V_{bseff}\right)}{K_1^{\,2}}}\right)$$

(c) Transition from linear to saturation region

A parameter Vcveff is used to smooth out the transition between linear and saturation regions. It affects the inversion charge.

(4.3.19)

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^{\,2} + 4\delta_4 V_{dsat,\,cv}}\right\} \quad where \quad V_4 = V_{dsat,cv} - V_{ds} - \delta_4; \quad \delta_4 = 0.02$$

(4.3.20)

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left(\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right) + \frac{A_{bulk}'^{\,2} V_{cveff}^{\,2}}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

Below is a list of all he three partitioning schemes for the inversion charge:

(4.3.21)

$$\delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}') A_{bulk}' V_{cveff}^{\,2}}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(i) The 50/50 Charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain nodes. Despite it's simplicity it is found to approximate the simulation data well.

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(4.3.22)

$$Q_s = Q_d = 0.5Q_{inv} = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

(ii) The 40/60 Channel-charge Partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain electrodes by assuming a linear dependence to the distance.

(4.3.23)

$$\begin{cases} Q_s = W_{active}\int_0^{L_{active}} q_c\left(1 - \frac{y}{L_{active}}\right)dy \\ Q_d = W_{active}\int_0^{L_{active}} q_c\frac{y}{L_{active}}dy \end{cases}$$

(4.3.24)

$$Q_s = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{4}{3}V_{gstefcvf}^2\left(A_{bulk}'V_{cveff}\right) + \frac{2}{3}V_{gsteff}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(4.3.25)

$$Q_d = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{5}{3}V_{gsteff\,cv}^2\left(A_{bulk}'V_{cveff}\right) + V_{gsteff\,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(iii) The 0/100 Charge Partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,cv}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{\left(A_{bulk}' V_{cveff}\right)^2}{24\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.26}$$

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,cv}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{\left(A_{bulk}' V_{cveff}\right)^2}{8\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.27}$$

(d) Bias dependent threshold voltage effects on capacitance

The effects of body bias and DIBL is included in the capacitance model by modifying the threshold voltage to make it consistent with the I-V model. In deriving the capacitances additional differentiations are need to account for the dependence of threshold voltage on drain and substrate biases. The intrinsic capacitances can be derived based on the above charge equations.

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(4.3.28)

$$C_{(s,d,g,b),g} = \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}}$$

(4.3.29)

$$C_{(s,d,g,b),s} = -\frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} + \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \left(\frac{\partial V_{th}}{\partial V_{ds}} + \frac{\partial V_{th}}{\partial V_{bs}} \right)$$

(4.3.30)

$$C_{(s,d,g,b),d} = \frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}cv} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{ds}}$$

(4.3.31)

$$C_{(s,d,g,b),b} = \frac{\partial Q_{s,d,g,b}}{\partial V_{bs}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}{}^{cv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{bs}}$$

4.4 Extrinsic Capacitance: Fringing Capacitance

The fringing capacitance consists of a bias independent outer fringing capacitance and a bias dependent inner fringing capacitance. In the present release only the bias independent outer fringing capacitance is implemented. Experimentally, it is virtually impossible to separate this capacitance with the overlap capacitance. Nonetheless, the outer fringing capacitance can be theoretically calculated:

(4.4.1)

$$CF = \frac{\varepsilon_{ox}}{\alpha} ln\left(1 + \frac{t_{poly}}{t_{ox}}\right) \qquad \alpha = \frac{\pi}{2}$$

If *CF* is not given in the above expression, it can be calculated by:

(4.4.2)

$$CF = \frac{2\varepsilon_{ox}}{\pi} ln\left(1 + \frac{4 \times 10^{-7}}{t_{ox}}\right)$$

4.5 Extrinsic Capacitance: Overlap Capacitance

An accurate model for the overlap capacitance is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap} = C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

(a) Source Overlap Charge

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(4.5.1)

$$\frac{Q_{overlap,s}}{W_{active}} = \text{CGS0}V_{gs} + \text{CGS1}\left\{V_{gs} - V_{gs,overlap} + \frac{\text{CKAPPA}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gs,overlap}}{\text{CKAPPA}}}\right)\right\}$$

(4.5.2)

$$V_{gs,overlap} = \frac{1}{2}\left\{\left(V_{gs} - \delta_1\right) + \sqrt{\left(V_{gs} - \delta_1\right)^2 - 4\delta_1}\right\} \quad where \quad \delta_1 = 0.02$$

where *CKAPPA* is a user input parameter. If the average doping in the LDD region is known, *CKAPPA* can be calculated by:

$$\frac{2e_{Si}qN_{LDD}}{C_{ox}^{\ 2}}$$

The typical value for N_{LDD} is 5x1017 cm-3.

(b) Drain Overlap Charge

(4.5.3)

$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd} + \text{CGD1}\left\{V_{gd} - V_{gd,overlap} + \frac{\text{CKAPPA}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gd,overlap}}{\text{CKAPPA}}}\right)\right\}$$

(4.5.4)

$$V_{gd,overlap} = \frac{1}{2}\left\{\left(V_{gd} - \delta_2\right) + \sqrt{\left(V_{gd} - \delta_2\right)^2 - 4\delta_2}\right\} \quad where \quad \delta_2 = 0.02$$

(c) Gate Overlap Charge

(4.5.5)

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right)$$

In the above expressions, if *CGS0* and *CGD0* (the heavily doped S/D region to gate overlap capacitance) are not given, they are calculated according to the following:

CGS0 = (*DLC*Cox)* - *CGS1* (if *DLC* is given and *DLC* > *0*)

CGS0 = 0 (if the previously calculated *CGS0* is less than 0)

CGS0 = 0.6 *Xj*Cox* (otherwise)

CGD0 = (*DLC*Cox)* - *CGD1* (if *DLC* is given and *DLC* > *CGD1/Cox*)

CGD0 = 0 (if previously calculated *CDG0* is less than 0)

CGD0 = 0.6 *Xj*Cox* (otherwise)

4.6 Graphical Results

Figures 4-1 through 4-4 are included to show the good behavior of the expressions introduced in this chapter. Note that both capacitance and charge are continuous under both Vds bias ranges (linear to saturation) and Vgs bias conditions (subthreshold to strong inversion). Figure 4-5 is also included to highlight the VFBeff equation used to ensured this continuity.

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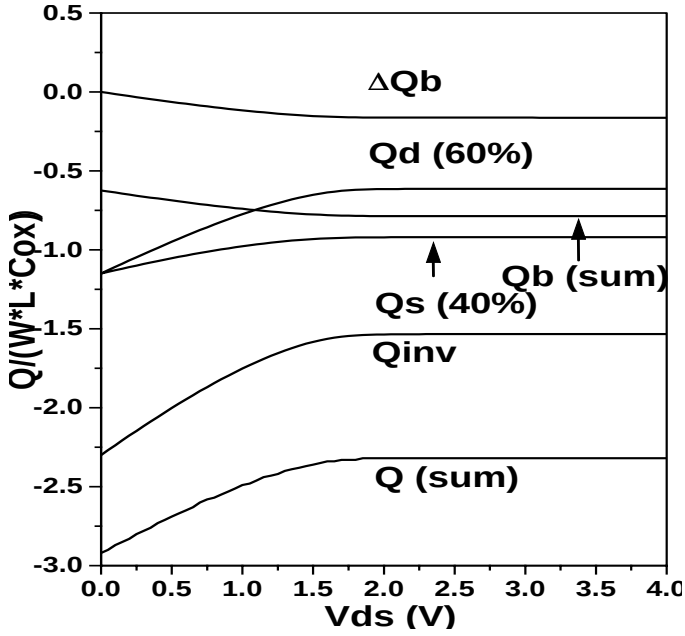

Figure 4-1. Normalized charge versus Vds bias.

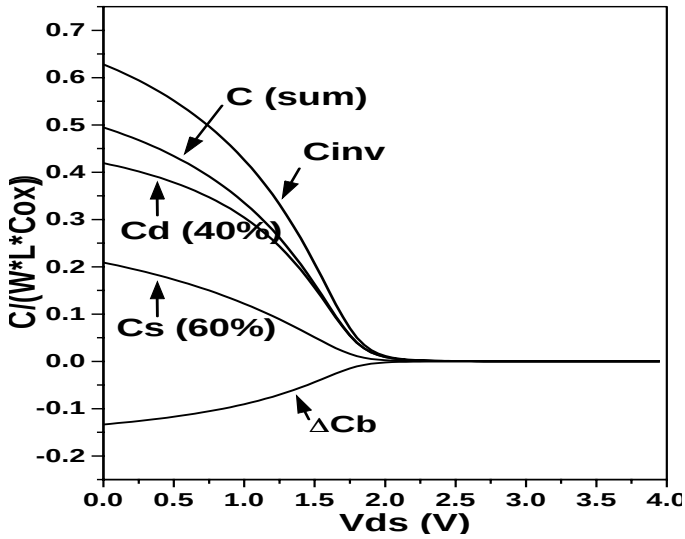

Figure 4-2. Normalized capacitance versus Vds bias.

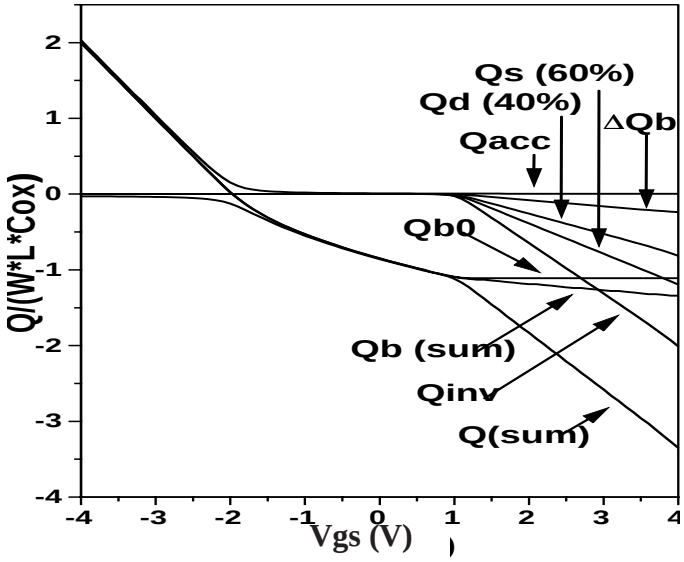

Figure 4-3. Normalized charge versus Vgs bias.

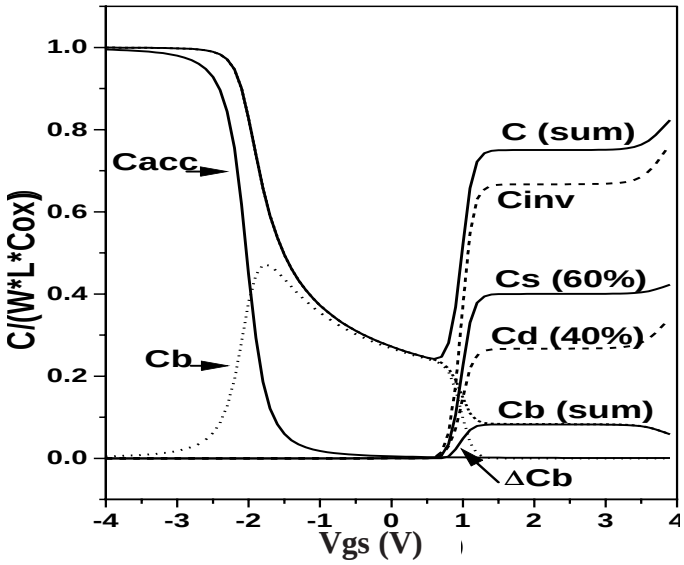

Figure 4-4. Normalized capacitance versus Vgs bias.

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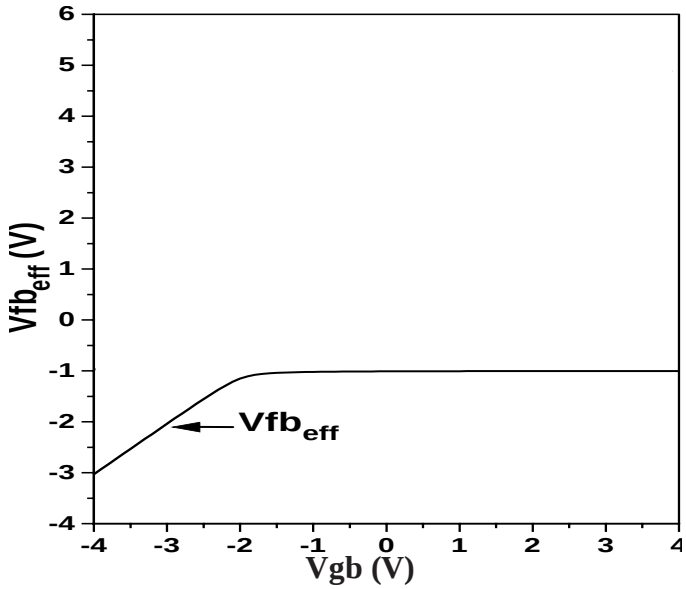

Figure 4-5. Continuity of the Vfbeff function.

CHAPTER 5: Non-Quasi Static Model

5.1 Background Information

As the MOS transistor becomes more performance-driven, the need to accurately predict circuit performance operating near device cut-off frequency becomes more essential as well. However, most device models available in circuit simulators such as SPICE fall short this need. They include models which are formulated upon Quasi-Static (QS) assumptions. In other words, the finite charging time for the inversion layer is ignored. When these models are used with the common 40/60 charge partitioning option, unrealistically large drain current spikes frequently occur [31]. In addition, the inability of these models to accurately simulate channel charge re-distribution causes problems in fast switched-capacitor type circuits. Many Non-Quasi-Static (NQS) models have been published, but these models have two shortcomings: 1) they assume, unrealistically, no velocity saturation, and 2) They are complex in their formulations; intuitive insights into NQS effects and solutions are lost. In addition, these models increase circuit simulation times by 4 to 5 times.

5.2 The NQS Model in BSIM3v3

BSIM3v3 includes a physical NQS transient model which alleviates the above problems. Although it is a physical model that takes in account velocity saturation

effects, it is conceptually simple to understand because its formulation is based on familiar channel relaxation principles.

5.3 Model Formulation

The channel of a MOSFET is analogous to a bias dependent RC distributed transmission line (Figure 5-1a). In the Quasi-Static (QS) approach, the gate capacitor node is lumped with both the external source and drain nodes (Figure 5-1b). This ignores the finite time for the channel charge to build-up. One Non-Quasi-Static (NQS) solution is to represent the channel as *n* transistors in series (Figure 5-1c). This model, although accurate, comes at the expense of simulation time. BSIM3v3 uses a more efficient approach formulated from the circuit of Figure 5-1d. This Elmore equivalent circuit models channel charge build-up accurately because it retains the lowest frequency pole of the original RC network (Figure 5-1a). To accommodate this new NQS model, two new parameters are introduced (See Table 5-1).

Name	Function	Default	Unit
NQSMOD	Flag for the NQS model	0	(False)
ELM	Elmore constant of the channel	5	none

Table 5-1. New NQS model parameters.

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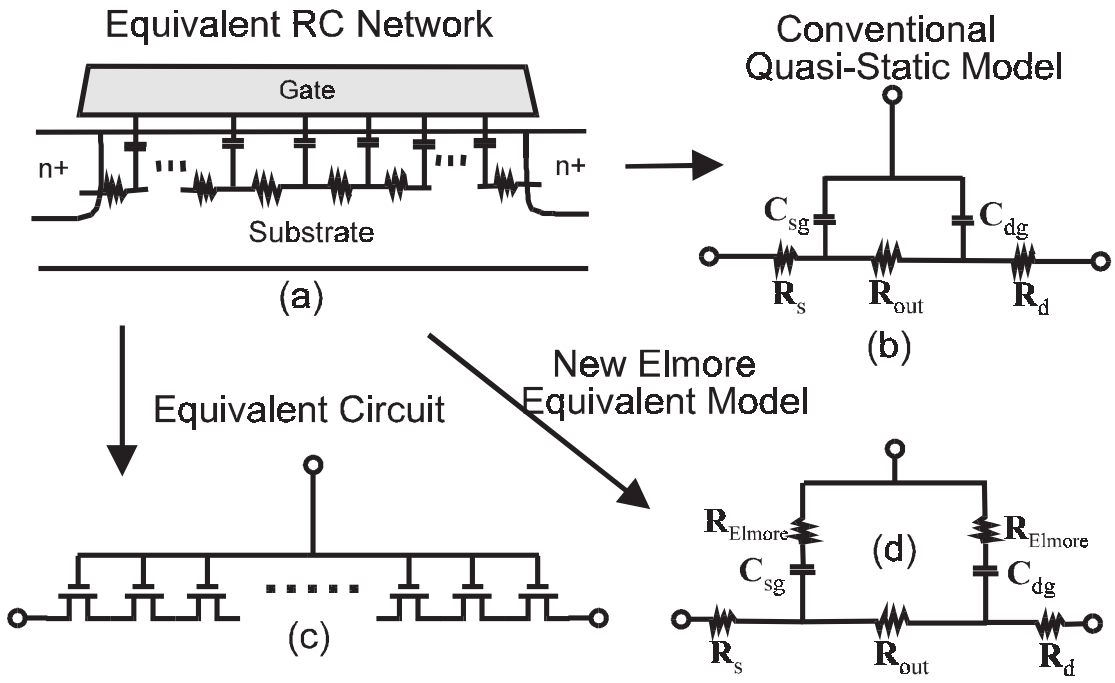

Figure 5-1. Quasi-Static and Non-Quasi-Static models for SPICE transient analysis.

The NQS model also includes the use of the model parameter Xpart (usually associated with the A.C. model) to control charge partition to the source/drain. In BSIM3v3, the Elmore resistance, R_{Elmore}, is calculated from the channel resistance under strong inversion as:

(5.2.1)

$$R_{Elmore} = \frac{L_{eff}^2}{\varepsilon \mu_{eff} Q_{ch}} \approx \frac{L_{eff}^2}{\varepsilon \mu_{eff} Q_{cheq}}$$

where ε is the Elmore constant of the RC network in the channel with a theoretical value close to 5. Q_{ch} is the actual channel charge in the channel and Q_{cheq} represents the quasi-static equilibrium channel charge. The value $R_{Elmore}C_{Channel}$ is the relaxation time constant for charging and discharging the channel. Under strong inversion, the conduction is mainly due to drift current. As such, the relaxation time constant due to drift current is given by:

$$\tau_{drift} \approx R_{Elmore}C_{ox}W_{eff}L_{eff} \approx \frac{C_{ox}W_{eff}L_{eff}^{3}}{\varepsilon\mu_{eff}Q_{cheq}} \tag{5.2.2}$$

Under weak inversion, conduction is mainly due to diffusion current. The relaxation time constant can be approximated by:

$$\tau_{diff} \approx \frac{q(L_{eff}/4)^{3}}{\mu_{eff}kT} \tag{5.2.3}$$

The overall relaxation time for channel charging and discharging is given by the combination of both the diffusion and the drift terms:

$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{drift}} \tag{5.2.4}$$

Using this relaxation time concept, the NQS transient effect in BSIM3v3 is implemented with the subcircuit given in Figure 5-2. The parameters X_d and X_s are the charge partition allocated to the drain and source and are assigned values of 0.4 and 0.6, respectively.

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The state variable, Q_{def}, is an additional node created to keep track of the amount of deficit (or surplus) channel charge necessary to achieve equilibrium . Q_{def} will decay exponentially into the channel with a bias dependent NQS relaxation time τ. The derivative of Q_{def} with respect to time is the gate charging current. This gate current is partitioned into separate drain and source current components. A complete list of all NQS model equations is provided in the Appendix.

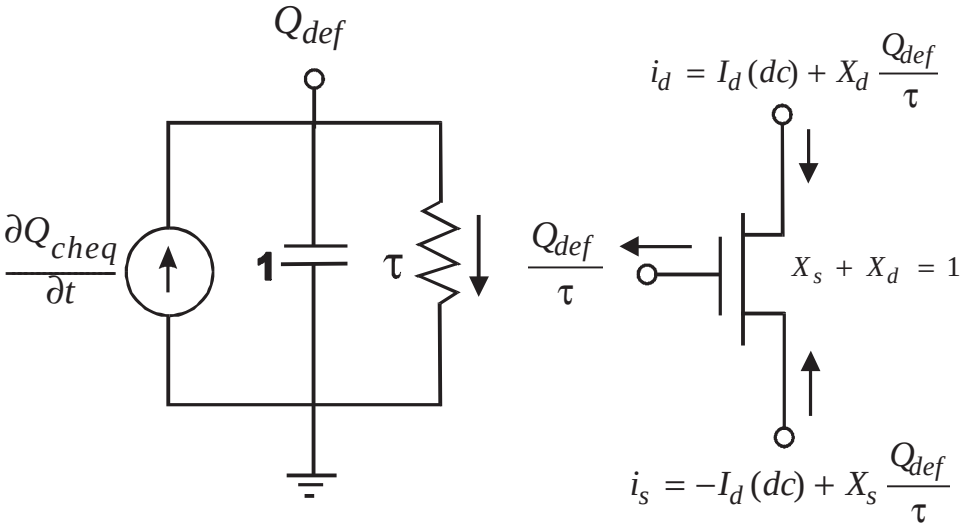

Figure 5-2. NQS subcircuit implementation in BSIM3v3.

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CHAPTER 6: Parameter Extraction

Parameter extraction is an important part of model development. Many different extraction methods have been developed [23, 24]. The appropriate methodology depends on the model and on the way the model is used. Based on the properties of the BSIM3v3, a combination of a local optimization and the group device extraction strategy is adopted for parameter extraction.

6.1 Optimization strategy

There are two main, different optimization strategies: global optimization and local optimization. Global optimization relies on the explicit use of a computer to find one set of model parameters which will best fit the available experimental (measured) data. This methodology may give the minimum average error between measured and simulated (calculated) data points, but it also treats each parameter as a "fitting" parameter. Physical parameters extracted in such a manner might yield values that are not consistent with their physical intent.

In local optimization, many parameters are extracted independently of one another. Parameters are extracted from device bias conditions which correspond to dominant physical mechanisms. Parameters which are extracted in this manner might not fit experimental data in all the bias conditions. Nonetheless, these extraction methodologies are developed specifically with respect to a given parameter’s physical meaning. If properly executed, it should, overall, predict

device performance quite well. Values extracted in this manner will now have some physical relevance.

6.2 Extraction Strategies

Two different strategies are available for extracting parameters: the single device extraction strategy and group device extraction strategy. In single device extraction strategy, experimental data from a single device is used to extract a complete set of model parameters. This strategy will fit one device very well but will not fit other devices with different geometries. Furthermore, single device extraction strategy can not guarantee that the extracted parameters are physical. If only one set of channel length and width is used, parameters related to channel length and channel width dependencies can not be determined.

BSIM3v3 uses group device extraction strategy. This requires measured data from devices with different geometries. All devices are measured under the same bias conditions. The resulting fit might not be absolutely perfect for any single device but will be better for the group of devices under consideration.

6.3 Extraction Procedure

6.3.1 Parameter Extraction Requirements

One large size device and two sets of smaller-sized devices are needed to extract parameters, as shown in Figure 6-1.

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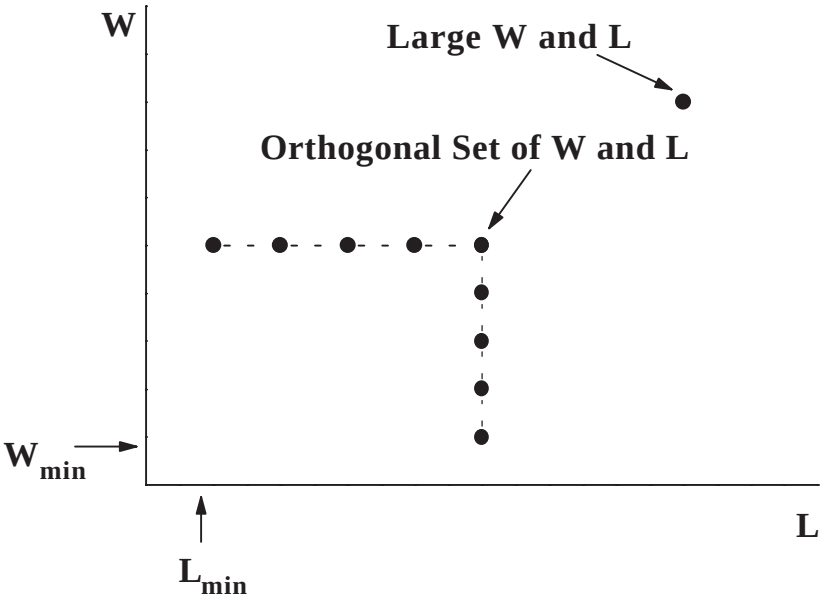

Figure 6-1. Device geometries used for parameter extraction

The large-sized device (W ≥ 10μm, L ≥ 10μm) is used to extract parameters which are independent of short/narrow channel effects and parasitic resistance. Specifically, these are: mobility, the large-sized device threshold voltage V_{Tideal}, and the body effect coefficients K_1 and K_2 which depend on the vertical doping concentration distribution. The set of devices with a fixed large channel width but different channel lengths are used to extract parameters which are related to the short channel effects. Similarly, the set of devices with a fixed, long channel length but different channel widths are used to extract parameters which are related to narrow width

effects. Regardless of device geometry, each device will have to be measured under four, distinct bias conditions.

1) I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ with different V_{bs}.

2) I_{ds} vs. V_{ds}@ $V_{bs} = 0V$ with different V_{gs}.

3) I_{ds} vs. V_{gs}@ $V_{ds} = V_{dd}$ with different V_{bs}. (V_{dd} is the maximum drain voltage)

4) I_{ds} vs. V_{ds}@ $V_{bs} = V_{bb}$ with different V_{gs}. ($|V_{bb}|$ is the maximum body bias)

6.3.2 Optimization

The optimization process recommended for BSIM3v3 is a combination of Newton-Raphson's iteration and linear-squares fit of either one, two, or three variables. This methodology was discussed by M. C. Jeng [18]. A flow chart of this optimization process is shown in Figure 6-2. The model equation is first arranged in a form suitable for Newton-Raphson's iteration as shown in Eq. (6.3.1):

$$f_{\exp}(P_{10},P_{20},P_{30}) - f_{sim}(P_1^{(m)},P_2^{(m)},P_3^{(m)}) = \frac{\partial f_{sim}}{\partial P_1}\Delta P_1^m + \frac{\partial f_{sim}}{\partial P_2}\Delta P_2^m + \frac{\partial f_{sim}}{\partial P_3}\Delta P_3^m \tag{6.3.1}$$

The variable $f_{sim}()$ is the objective function to be optimized. The variable $f_{exp}()$ stands for the experimental data. P_{10}, P_{20}, and P_{30} represent the desired extracted parameter values. $P_1^{(m)}$, $P_2^{(m)}$, and $P_3^{(m)}$ represent parameter values after the m*th* iteration.

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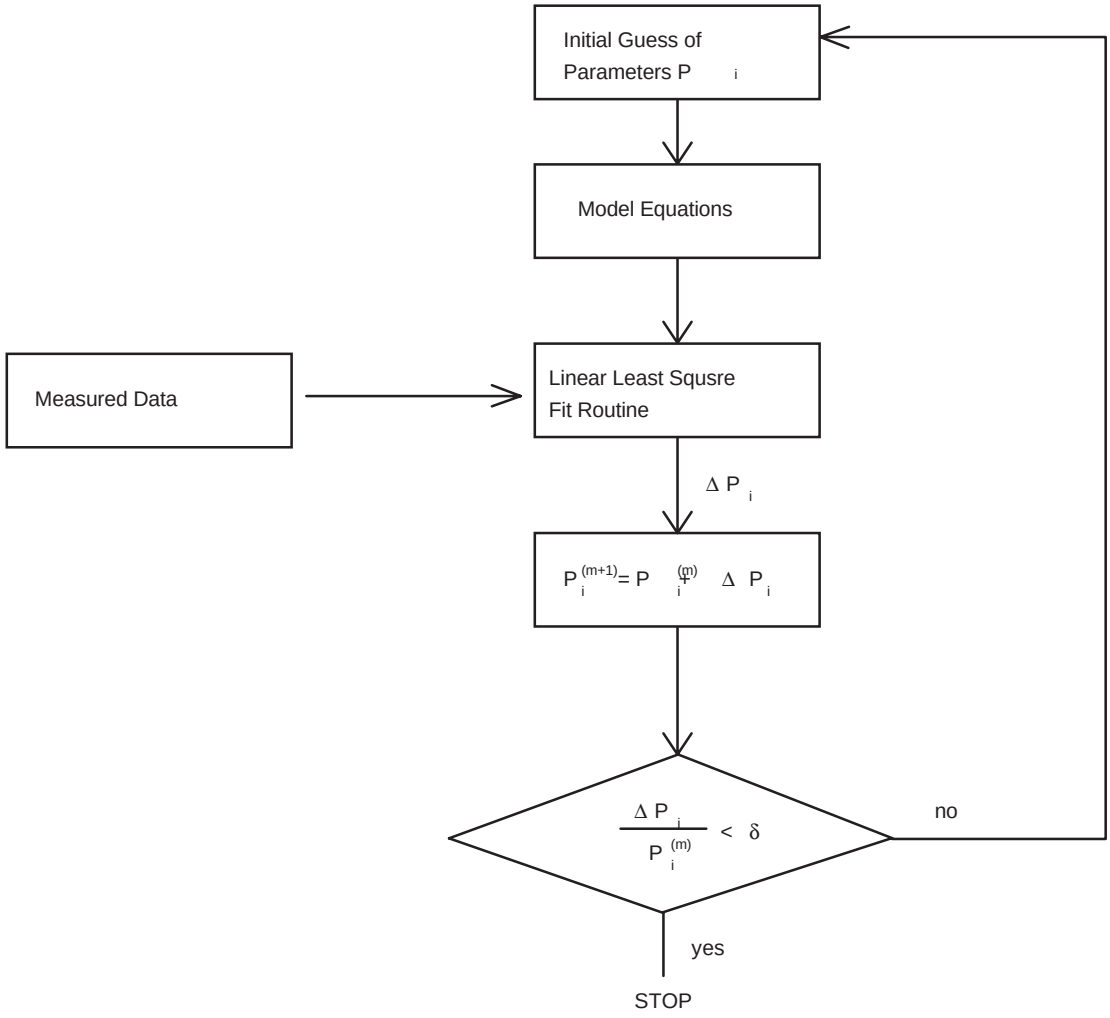

Figure 6-2. Optimization flow.

To change Eq. (6.3.1) into a form that a linear least-squares fit routine can be use (i.e. in a form of $y = a + bx1 + cx2$), both sides of the Eq. (6.3.1) are divided by $\partial f_{sim} / \partial P_1$. This gives the change in P_1, $\Delta P_1^{(m)}$, for the next iteration such that:

$$P_i^{(m+1)} = P_i^{(m)} + \Delta P_i^{(m)} \tag{6.3.2}$$

where i=1, 2, 3 for this example. The (m+1) parameter values for P2 and P3 are obtained in an identical fashion. This process is repeated until the incremental parameter change in parameter values $\Delta P_i^{(m)}$ are smaller than a pre-determined value. At this point, the parameters P_1, P_2, and P_3 have been extracted.

6.3.3 Extraction Routine

Before any model parameters can be extracted, some process parameters have to be provided. They are listed below in Table 6-1:

Input Parameters Names	Physical Meaning
T_{ox}	Gate oxide thickness
N_{ch}	Doping concentration in the channel
T	Temperature at which the data is taken
L_{drawn}	Mask level channel length
W_{drawn}	Mask level channel width
X_j	Junction depth

Table 6-1. Prerequisite input parameters prior to extraction process.

The parameters are extracted in the following procedure. These procedures are based on a physical understanding of the model and based on local

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optimization. (Note: *Fitting Target Data* refers to measurement data used for model extraction.)

Step 1

Extracted Parameters & Fitting Target Data	Device & Experimental Data
V_{th0}, K_1, K_2 Fitting Target Exp. Data: $V_{th}(V_{bs})$	Large Size Device (Large W & L). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs} Extracted Experimental Data $V_{th}(V_{bs})$

Step 2

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
μ_0, U_a, U_b, U_c Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	Large Size Device (Large *W* & *L*). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs}

Step 3

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
Lint, $R_{ds}(R_{dsw}, W, V_{bs})$ Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs}

Step 4

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$Wint$, $R_{ds}(R_{dsw}, W, V_{bs})$ Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs}

Step 5

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
R_{dsw}, $Prwb$, Wr Fitting Target Exp. Data: $R_{ds}(R_{dsw}, W, V_{bs})$	$R_{ds}(R_{dsw}, W, V_{bs})$

Step 6

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{vt0}, D_{vt1}, D_{vt2}, Nlx Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed W & Different L). $V_{th}(V_{bs}, L, W)$

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Step 7

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{vt0w}, D_{vt1w}, D_{vt2w} Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 8

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$K3$, $K3b$, W_0 Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 9

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
V_{off}, $Nfactor$, C_{dsc}, C_{dscb} Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs}

Step 10

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

C_{dscd} Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{ds} = Vbb$ at Different V_{ds}

Step 11

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
dWb Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ at Different V_{bs}

Step 12

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
v_{sat}, A_0, A_{gs} Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$ A_1, A_2 (PMOS Only) Fitting Target Exp. Data $V_{asat}(V_{gs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ at Different V_{gs}

Step 13

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

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B0, B1 Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *L* & Different *W*). I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ at Different V_{gs}

Step 14

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
dWg Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *L* & Different *W*). I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ at Different V_{gs}

Step 15

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
P_{scbe1}, P_{scbe2} Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ at Different V_{gs}

Step 16

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
P_{clm}, $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$, *Pavg* Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ at Different V_{gs}

Step 17

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{rout}, P_{dibl1c}, P_{diblc2} Fitting Target Exp. Data: $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$	One Set of Devices (Large and Fixed W & Different L). $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$

Step 18

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$P_{dibl1cb}$ Fitting Target Exp. Data: $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ fixed V_{gs} at Different V_{bs}

Step 19

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$\theta_{dibl}(Eta0, Etab, Dsub, L)$ Fitting Target Exp. Data: *Subthreshold region* $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

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Step 20

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
Eta0, Etab, Dsub Fitting Target Exp. Data: $\theta_{dibl(Eta0, Etab, L)}$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

Step 21

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
Keta Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{gs}

Step 22

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$\alpha 0$, $\beta 0$ Fitting Target Exp. Data: $I_{sub}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{ds}

6.4 Notes on Parameter Extraction

6.4.1 Parameters with Special Notes

Below is a list of model parameters which have special notes for parameter extraction.

Symbols used in SPICE	Description	Default Value	Unit	Notes
vth0	Threshold voltage for large W and L device @ Vbs=0V	0.7 (NMOS) -0.7 (PMOS)	V	nI-1
k1	First order body effect coefficient	0.5	$V^{1/2}$	nI-2
k2	Second order body effect coefficient	0	none	nI-2
vbm	Maximum applied body bias	-3	V	nI-2
nch	Channel doping concentration	1.7E17	$1/cm^3$	nI-3
gamma1	Body-effect coefficient near interface	calculated	$V^{1/2}$	nI-4
gamma2	Body-effect coefficient in the bulk	calculated	$V^{1/2}$	nI-5
vbx	Vbs at which the depletion width equals xt	calculated	V	nI-6
cgso	Non-LDD source-gate overlap capacitance per channel length	calculated	F/m	nC-1
cgdo	Non-Ldd drain-gate overlap capacitance per channel length	calculated	F/m	nC-2
cf	Fringing field capacitance	calculated	F/m	nC-3

Table 6-2. Parameters with notes for extraction.

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6.4.2 Explanation of Notes

nI-1. If Vtho is not specified, it is calculated using:

$$V_{tho} = V_{FB} + \phi_s + K_1\sqrt{\phi_s}$$

where VFB=-1.0. If Vth0 is specified, VFB is calculated using

$$V_{FB} = V_{tho} - \phi_s - K_1\sqrt{\phi_s}$$

nI-2. If k1 and k2 are not given, they are calculated using:

$$K_1 = gamma_2 - 2K_2\sqrt{\phi_s - V_{bm}}$$

$$K_2 = \frac{(gamma1 - gamma2)(\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

where the parameter phi is calculated using:

$$\phi_s = 2v_{tm0}\,ln\left(\frac{Nch}{ni}\right)$$

$$v_{tm0} = \frac{k_B T_{nom}}{q}$$

$$n_i = 1.45x10^{10}\left(\frac{T_{nom}}{300.15}\right)^{1.5} exp\left(21.5565981 - \frac{E_{g0}}{2v_{tm0}}\right)$$

$$E_{g0} = 1.16 - \frac{7.02x10^{-4} T_{nom}^{2}}{T_{nom} + 1108}$$

where E_{g0} is the energy bandgap at temperature Tnom.

nI-3. If nch is not given and gamma1 is given, nch is calculated from:

$$N_{ch} = \frac{gamma1^2 C_{ox}^2}{2q\varepsilon_{si}}$$

If both gamma1 and nch are not given, nch defaults to 1.7e23 $1/m^3$ and gamma1 is calculated from nch.

nI-4. If gamma1 is not given, it is calculated using:

$$gamma_1 = \frac{\sqrt{2q\varepsilon_{si} N_{ch}}}{C_{ox}}$$

nI-5. If gamma2 is not given, it is calculated using:

$$gamma_2 = \frac{\sqrt{2q\varepsilon_{si} N_{sub}}}{C_{ox}}$$

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nI-6. If vbx is not given, it is calculated using:

$$V_{bx} = \phi_s - \frac{qN_{ch}X_t^2}{2\varepsilon_{si}}$$

nC-1. If cgso is not given then it is calculated using:

if (dlc is given and is greater 0) then,

cgso = p1 = (dlc*cox) - cgs1

if (the previously calculated cgso <0), then

cgso=0

else cgso = 0.6 xj*cox

nC-2. If cgdo is not given then it is calculated using:

if (dlc is given and is greater than 0) then,

cgdo = p2 = (dlc*cox) - cgd1

if (the previously calculated cgdo <0), then

cgdo=0

else cgdo = 0.6 xj*cox

nC-3. If cf is not given then it is calculated using:

$$CF = \frac{2\varepsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{Tox}\right)$$

CHAPTER 7: Benchmark Test Results

A series of tests [26] have been performed on BSIM3v3 to check its robustness (lack of discontinuities), accuracy, and performance. Although all benchmark test results could not be included in this chapter, the most important ones will be presented in this chapter for a 0.5μm, 90 Angstrom, 3.3V technology.

7.1 Benchmark Test Types

Table 7-1 lists the various benchmark tests and its associated figure number included in this section. Notice that for each plot, smooth transitions are apparent for current, transconductance, and source to drain resistance for all transition regions regardless of bias conditions.

Device Size	Bias Conditions	Notes	Figure Number
W/L=20/5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Log scale	7-1
W/L=20/5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Linear scale	7-2
W/L=20/0.5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Log scale	7-3
W/L=20/0.5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Linear scale	7-4
W/L=20/5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Log scale	7-5
W/L=20/5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V; W/L=20/5	Linear scale	7-6
W/L=20/0.5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Log scale	7-7

Device Size	Bias Conditions	Notes	Figure Number
W/L=20/0.5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Linear scale	7-8
W/L=20/5	Gm/Ids vs. Vgs @ Vds=0.05V, 3-3V; Vbs=0V	Linear scale	7-9
W/L=20/0.5	Gm/Ids vs. Vgs @ Vds=0.05V, 3-3V; Vbs=0V	Linear scale	7-10
W/L=20/5	Gm/Ids vs. Vgs @ Vds=0.05V; Vbs=0V to -3.3V	Linear scale	7-11
W/L=20/0.5	Gm/Ids vs. Vgs @ Vds=0.05V; Vbs=0V to -3.3V	Linear scale	7-12
W/L=20/0.5	Ids vs. Vds @Vbs=0V; Vgs=0.5V, 0.55V, 0.6V	BSIM3 Version 2.0 vs. BSIM3v3	7-13
W/L=20/5	Ids vs. Vds @Vbs=0V; Vgs=1.15V to 3.3V	Linear scale	7-14
W/L=20/0.5	Ids vs. Vds @Vbs=0V; Vgs=1.084V to 3.3V	Linear scale	7-15
W/L=20/0.5	Rout vs. Vds @ Vbs=0V; Vgs=1.084V to 3.3V	Linear scale	7-16

Table 7-1. Benchmark tests.

7.2 Benchmark Test Results (Figures)

All of the figures listed in Table 7-1 will now be listed in order. Unless indicated otherwise, symbols represent actual data and lines represent the results of BSIM3v3 calculations. All of these plots serve to demonstrate the robustness and continuous behavior of the unified model expression for not only Ids but Gm, Gm/Ids, and Rout as well.

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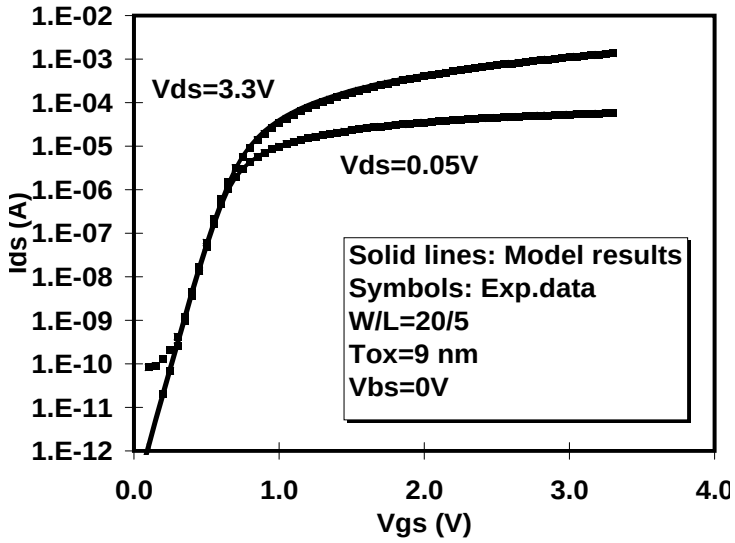

Figure 7-1. Continuity from subthreshold to strong inversion (log scale).

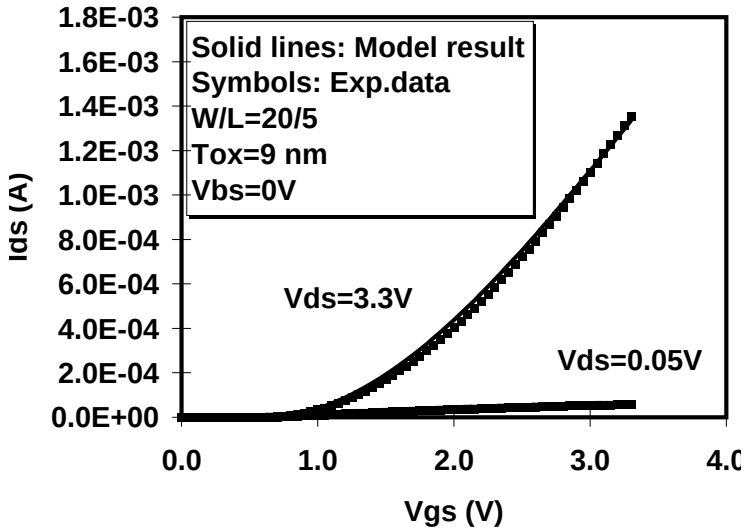

Figure 7-2. Continuity from subthreshold to strong inversion (linear scale).

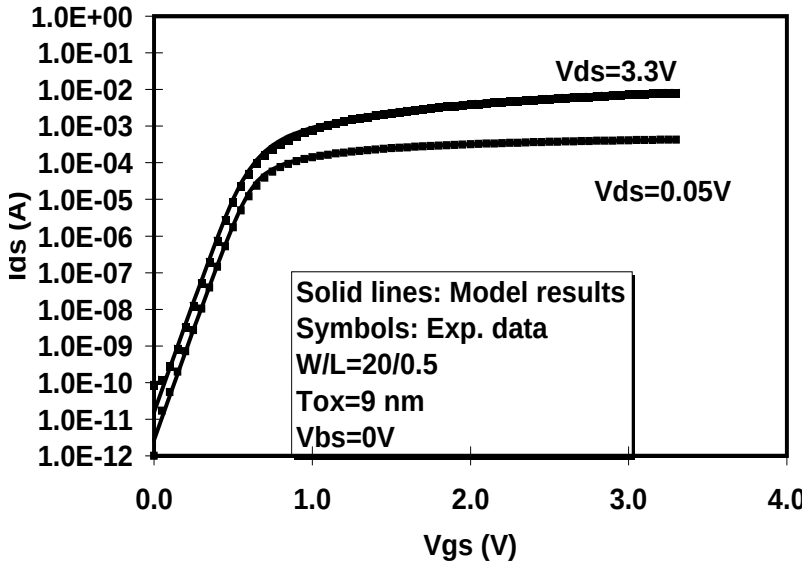

Figure 7-3. Same as Figure 7-1 but for short channel device.

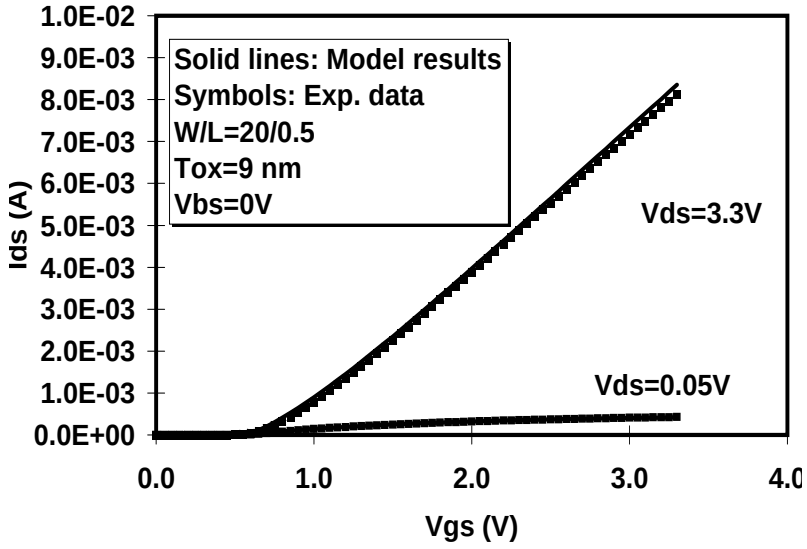

Figure 7-4. Same as Figure 7-2 but for short channel device.

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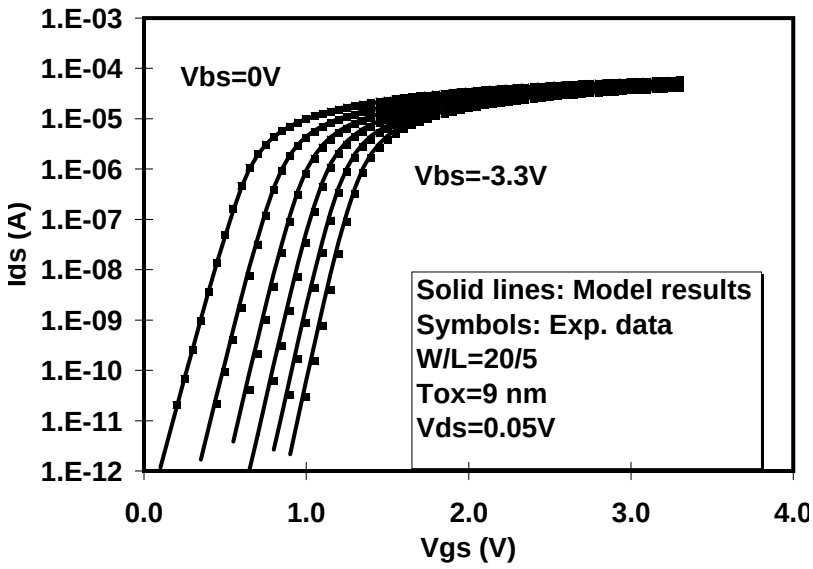

Figure 7-5. Subthreshold to strong inversion continuity as function of Vbs.

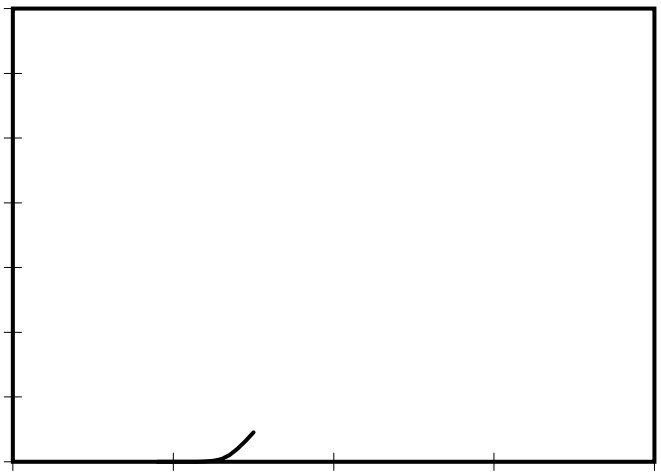

Figure 7-6. Subthreshold to strong inversion continuity as function of Vbs.

CHAPTER 8: Noise Model

8.1 Flicker Noise

8.1.1 Parameters

There exists two models for flicker noise. One is called as Spice2 flicker noise model, another one is called as BSIM3 flicker noise model [33,34]. The parameters in the models are listed in Table 8-1.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none
Em	em	Saturation field	4.1e7	V/m
Af	af	Frequency exponent	1	none
Ef	ef	Flicker exponent	1	none
Kf	kf	Flicker noise parameter	0	none

Table 8-1. Flicker Noise Model Parameters.

8.1.2 Expressions

1. For Spice2 model

$$Flicker\ Noise = \frac{K_f I_{ds}^{af}}{C_{ox} L_{eff}^{2} f^{ef}} \tag{8.1a}$$

2. For BSIM3v3 model

1.1) If Vgs>Vth+0.1:

$$Flicker\ Noise = \frac{vtq^2 I_{ds}\mu_{eff}}{f^{Ef} L_{eff}^{2} C_{ox} 10^8}[N_{oia}\log(\frac{No + 2x10^{14}}{Nl + 2x10^{14}}) + N_{oib}(No - Nl) + 0.5N_{oic}(No^2 - Nl^2)] + \frac{vtI_{ds}^{2}\Delta L_{clm}}{f^{Ef} L_{eff}^{2} W_{eff} 10^8}\frac{N_{oia} + N_{oib}Nl + N_{oic}Nl^2}{(Nl + 2x10^{14})^2} \tag{8.1b}$$

where V_{tm} is the thermal voltage, μ_{eff} is the effective mobiity at the given bias condition, L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source given by:

$$N_0 = \frac{C_{ox}(V_{GS} - V_{TH})}{q} \tag{8.2}$$

The parameter N_l is the charge density at the drain given by:

$$N_l = \frac{C_{ox}(V_{GS} - V_{TH} - V_{DS}')}{q} \tag{8.3}$$

$$V_{DS}' = MIN(V_{DS}, V_{DSAT})$$

ΔLclm refers to channel length reduction due to CLM and is given by:

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(8.4)

$$\Delta L_{clm} = \begin{cases} Litl \times \log\left(\dfrac{\dfrac{V_{DS}-V_{DSAT}}{Litl}+Em}{E_{SAT}}\right) & \text{if VDS > VDSAT} \\ 0 & \text{otherwise} \end{cases}$$

$$E_{SAT} = \frac{2 \times Vsat}{u_{eff}}$$

2. Otherwise,

(8.5)

$$FlickerNoise = \frac{S_{limit} \times S_{wi}}{S_{limit} + S_{wi}}$$

Where, S_{limit} is the flicker noise calculated at Vgs=Vth+0.1 and S_{wi} is given by:

(8.6)

$$Swi = \frac{Noia\,VtIds^2}{WeffLeff \quad f^{Ef}\, 4x10^{36}}$$

8.2 Channel Thermal Noise

There also exists two models for channel thermal noise. One is called as Spice2 thermal noise model. Another one is called as BSIM3v3 thermal noise model. Each of these can be toggled by the **noimod** flag.

1. For Spice2 thermal noise model

$$\frac{8kT}{3}(gm + gds + gmb)$$

2. For BSIM3v3 thermal noise model

$$\frac{4KT\mu_{eff}}{L_{eff}{}^2}|Q_{inv}|$$

$$Q_{inv} = -W_{eff} L_{eff} C_{ox} V_{gsteff} (1 - \frac{A_{bulk}}{2(V_{gsteff} + 2vt)} V_{dseff})$$

The derivation for this last thermal noise expression is based on the noise model found in [35].

8.3 Noise Model Flag

The **noimod** flag is used to select different combination of flicker and thermal noise models discussed above, as given in Table 8.2.

noimod flag	Flicker noise model	Thermal noise model
1	Spice2	Spice2
2	BSIM3v3	BSIM3v3
3	BSIM3v3	Spice2
4	Spice2	BSIM3v3

Table 8-2. Noimod flag for differnet noise models

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CHAPTER 9: MOS Diode Model

9.1 MOS Diode DC Current Model

9.1.1 Model Equations

9.1.1.1 Source/bulk Diode

If the saturation current Isbs is larger than zero, the following equations is used to calculate the source/bulk diode current:

Vbs<0.5V

(9.1.1)

$$I_{bs} = I_{sbs}[\exp(\frac{V_{bs}}{N\nu_{tm}}) - 1] + G_{\min} V_{bs}$$

V_{bs}>0.5V

(9.1.2)

$$I_{bs} = I_{sbs}[\exp(\frac{0.5}{N\nu_{tm}}) - 1] + \frac{I_{sbs}}{N\nu_{tm}} \exp(\frac{0.5}{N\nu_{tm}})(V_{bs} - 0.5) + G_{\min} V_{bs}$$

Where $N\nu tm=njKT/q$, nj is the emission coefficient of the source junction, and Isbs is calculated by

(9.1.3)

$$I_{sbs} = A_s J_s + P_s J_{ssw}$$

where Js is the saturation current density of the source/bulk diode, A_S is the area of the source junction. Jssw is the sidewall saturation current density of the source/bulk diode, Ps is the perimeter of the source junction. Js and Jssw are functions of temperature and can be described by:

(9.1.4a)

$$J_s = J_{s0} \exp[\frac{\frac{E_{g0}}{V_{tm0}} - \frac{E_g}{V_{tm}} + XTI \ln(\frac{T}{T_{nom}})}{N_j}]$$

(9.1.4b)

$$J_{ssw} = J_{s0sw} exp[\frac{\frac{E_{g0}}{V_{tm0}} - \frac{E_g}{V_{tm}} + XTI\, ln(\frac{T}{T_{nom}})}{N_j}]$$

(9.1.5)

$$E_g = 1.16 - \frac{7.02e^{-4}T^2}{T + 1108.0}$$

where Js0 is the saturation current density at Tnom. If Js0 is not given in the simulation, Js0=1.e-4A/m^2. Js0sw is the sidewall saturation current density at Tnom. The default value of Js0sw is 0.

If Isbs is less than zero, the source/bulk diode current is calculated by

(9.1.6)

$$I_{bs} = G_{\min} V_{bs}$$

9.1.1.2 Drain/bulk Diode

If the saturation current Isbd is larger than zero, the following equations is used to calculate the drain/bulk diode current:

Vbd<0.5V

(9.1.7)

$$I_{bd} = I_{sbd}[\exp(\frac{V_{bd}}{N\nu_{tm}}) - 1] + G_{\min} V_{bd}$$

V_{bd}>0.5V

(9.1.8)

$$I_{bd} = I_{sbd}[\exp(\frac{0.5}{N\nu_{tm}}) - 1] + \frac{I_{sbd}}{N\nu_{tm}} \exp(\frac{0.5}{N\nu_{tm}})(V_{bd} - 0.5) + G_{\min} V_{bd}$$

Where *Nvtm=njKT/q*, nj is the emission coefficient of the drain junction, and Isbd is calculated by

(9.1.9)

$$I_{sbd} = J_s A_D + J_{ssw} P_D$$

where Js is the saturation current density of the drain/bulk diode, A_D is the area of the drain junction. Jssw is the sidewall saturation current density of the drain/bulk diode, P_D is the perimeter of the drain junction. Js and Jssw are functions of temperature and given by (9.1.4a), (9.1.4b) and (9.1.5).

If Isbd is less than zero, the drain/bulk diode current is calculated by

(9.1.10)

$$I_{sbd} = G_{\min} V_{bd}$$

9.1.2 Parameters

The parameters for the DC model of the source/drain diode are listed in Table 9-1.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Js0	js	Saturation current density	1.e-4	A/m^2
Js0sw	jssw	Side wall saturation current density	0	A/m
nj	nj	Emission coefficient	1	none
XTI	xti	Junction current temperature exponent coefficient	3.0	none

Table 9-1. MOS Diode Model Parameters.

9.2 MOS Diode Capacitance Model

9.2.1 Model Equations

Source and drain junction capacitance can be divided into two components: the junction bottom area capacitance Cjb and the junction periphery capacitance Cjp. The formula for both the capacitances is similar, but with different model parameters. The equation of Cjb includes the parameters such as Cj, Mj, and Pb. The equation of Cjp includes the parameters such as Cjsw, Mjsw, Pbsw, Cjswg, Mjswg, Pbswg.

9.2.1.1 Source/bulk Junction Capacitance

The source/bulk junction capacitance can be calculated by:

If Ps >Weff

(9.2.1a)

$$Capbs = A_S C_{jbs} + (P_S - W_{eff}) C_{jbssw} + W_{eff} C_{jbsswg}$$

Otherwise:

(9.2.1b)

$$Capbs = A_S C_{jbs} + P_S C_{jbsswg}$$

where Cjbs is the bottom area capacitance of the source/bulk junction, Cjbssw is the periphery capacitance of the source/bulk junction along the field oxide side, and Cjbsswg is the periphery capacitance of the source/bulk junction along the gate oxide side.

If Cj is larger than zero, Cjbs is calculated by:

if Vbs<0

(9.2.2)

$$C_{jbs} = C_j(1 - \frac{V_{bs}}{P_b})^{-M_j}$$

if Vbs>0

(9.2.3)

$$C_{jbs} = C_j(1 + M_j \frac{V_{bs}}{P_b})$$

If Cjsw is large than zero, Cjbssw is calculated by:

if Vbs<0

(9.2.4)

$$C_{jbssw} = C_{jsw}(1 - \frac{V_{bs}}{P_{bsw}})^{-Mswj}$$

if Vbs>0

(9.2.5)

$$C_{jbssw} = C_{jsw}(1 + M_{jsw}\frac{V_{bs}}{P_{bsw}})$$

If Cjswg is larger than zero, Cjbsswg is calculated by:

if Vbs<0

(9.2.6)

$$C_{jbsswg} = C_{jswg}(1 - \frac{V_{bs}}{P_{bswg}})^{-Mjswg}$$

if Vbs>0

(9.2.7)

$$C_{jbsswg} = C_{jswg}(1 + M_{jswg}\frac{V_{bs}}{P_{bswg}})$$

9.2.1.2 Drain/bulk Junction Capacitance

The drain/bulk junction capacitance can be calculated by:

If P_D > Weff:

(9.2.8a)

$$Capbd = A_D C_{jbd} + (P_D - W_{eff}) C_{jbdsw} + W_{eff} C_{jbdswg}$$

Otherwise:

(9.2.8b)

$$Capbd = A_D C_{jbd} + P_D C_{jbdswg}$$

where Cjbd is the bottom area capacitance of the drain/bulk junction, Cjbdsw is the periphery capacitance of the drain/bulk junction along the field oxide side, and Cjbdswg is the periphery capacitance of the drain/bulk junction along the gate oxide side.

If Cj is larger than zero, Cjbd is calculated by:

if Vbd<0

(9.2.9)

$$C_{jbd} = C_j (1 - \frac{V_{bd}}{P_b})^{-M_j}$$

if Vbd>0

(9.2.10)

$$C_{jbd} = C_j (1 + M_j \frac{V_{bd}}{P_b})$$

if Cjsw is larger than zero, Cjbdsw is calculated by:

if Vbd<0

(9.2.11)

$$C_{jbdsw} = C_{jsw}(1 - \frac{V_{bd}}{P_{bsw}})^{-Mswj}$$

if Vbd>0

(9.2.12)

$$C_{jbdsw} = C_{jsw}(1 + M_{jsw}\frac{V_{bd}}{P_{bsw}})$$

if Cjswg is larger than zero, Cjbdswg is calculated by:

if Vbd<0

(9.2.13)

$$C_{jbdswg} = C_{jswg}(1 - \frac{V_{bd}}{P_{bswg}})^{-Mjswg}$$

if Vbd>0

(9.2.14)

$$C_{jbdswg} = C_{jswg}(1 + M_{jswg}\frac{V_{bd}}{P_{bswg}})$$

9.2.2 Parameters

The parameters for the capacitance model of the source/drain diode are listed in Table 9-2.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Cj	cj	Bottom junction capacitance per unit area at zero bias	5e-4	F/m^2
Mj	mj	Bottom junction capacitance grading coefficient	0.5	none
Pb	pb	Bottom junction built-in potential	1.0	V
Cjsw	cjsw	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias	5e-10	F/m
Mjsw	mjsw	Source/drain sidewall junction capacitance grading coefficient	0.33	none
Pbsw	pbsw	Source/drain sidewall junction built-in potential	1.0	V
Cjswg	cjswg	Source/drain gate sidwall junction capacitance per unit length at zero bias	Cjsw	F/m
Mjswg	mjswg	Source/drain gate sidewall junction capacitance grading coefficient	Mjsw	none
Pbswg	pbswg	Source/drain gate sidewall junction built-in potential	Pbsw	V

Table 9-2. MOS Diode Capacitance Model Parameters.

APPENDIX A: Parameter List

A.1 BSIM3v3 Model Control Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
none	level	BSIMv3 model selector	8	none	
Mobmod	mobmod	Mobility model selector	1	none	
Capmod	capmod	Flag for the short channel capacitance model	2	none	
Nqsmod	nqsmod	Flag for NQS model	0	none	
Noimod	noimod	Flag for noise model	1	none	

A.2 DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Vth0	vth0	Threshold voltage @Vbs=0 for Large L.	0.7 (NMOS) -0.7 (PMOS)	V	nI-1
K1	k1	First order body effect coeffi-cient	0.5	$V^{1/2}$	nI-2

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
K2	k2	Second order body effect coefficient	0.0	none	nI-2
K3	k3	Narrow width coefficient	80.0	none	
K3b	k3b	Body effect coefficient of k3	0.0	1/V	
W0	w0	Narrow width parameter	2.5e-6	m	
Nlx	nlx	Lateral non-uniform doping parameter	1.74e-7	m	
Vbm	vbm	Maximum applied body bias in Vth calculation	-3.0	V	
Dvt0	dvt0	first coefficient of short-channel effect on Vth	2.2	none	
Dvt1	dvt1	Second coefficient of short-channel effect on Vth	0.53	none	
Dvt2	dvt2	Body-bias coefficient of short-channel effect on Vth	-0.032	1/V	
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	0	1/m	
Dvt1w	dvtw1	Second coefficient of narrow width effect on Vth for small channel length	5.3e6	1/m	
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	-0.032	1/V	
$\mu 0$	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	 670.0 250.0	$cm^2/V/sec$	

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Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Ua	ua	First-order mobility degradation coefficient	2.25E-9	m/V	
Ub	ub	Second-order mobility degradation coefficient	5.87E-19	$(m/V)^2$	
Uc	uc	Body-effect of mobility degradation coefficient	mobmod =1, 2: -4.65e-11 mobmod =3: -0.046	m/V^2 1/V	
vsat	vsat	Saturation velocity at Temp = Tnom	8.0E4	m/sec	
A0	a0	Bulk charge effect coefficient for channel length	1.0	none	
Ags	ags	gate bias coefficient of Abulk	0.0	1/V	
B0	b0	Bulk charge effect coefficient for channel width	0.0	m	
B1	b1	Bulk charge effect width offset	0.0	m	
Keta	keta	Body-bias coefficient of bulk charge effect	-0.047	1/V	
A1	a1	First non-saturation effect parameter	0.0	1/V	
A2	a2	Second non-saturation factor	1.0	none	
Rdsw	rdsw	Parasitic resistance per unit width	0.0	Ω-μm^{Wr}	
Prwb	prwb	Body effect coefficient of Rdsw	0	$V^{-1/2}$	
Prwg	prwg	Gate bias effect coefficient of Rdsw	0	1/V	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Wr	wr	Width Offset from Weff for Rds calculation	1.0	none	
Wint	wint	Width offset fitting parameter from I-V without bias	0.0	m	
Lint	lint	Length offset fitting parameter from I-V without bias	0.0	m	
dWg	dwg	Coefficient of Weff's gate dependence	0.0	m/V	
dWb	dwb	Coefficient of Weff's substrate body bias dependence	0.0	$m/V^{1/2}$	
Voff	voff	Offset voltage in the subthreshold region at large W and L	-0.08	V	
Nfactor	nfactor	Subthreshold swing factor	1.0	none	
Eta0	eta0	DIBL coefficient in subthreshold region	0.08	none	
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect	-0.07	1/V	
Dsub	dsub	DIBL coefficient exponent in subthreshold region	drout	none	
Cit	cit	Interface trap capacitance	0.0	F/m^2	
Cdsc	cdsc	Drain/Source to channel coupling capacitance	2.4E-4	F/m^2	
Cdscb	cdscb	Body-bias sensitivity of Cdsc	0.0	F/Vm^2	
Cdscd	cdscd	Drain-bias sensitivity of Cdsc	0.0	F/Vm^2	
Pclm	pclm	Channel length modulation parameter	1.3	none	

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Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	0.39	none	
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	0.0086	none	
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	0	1/V	
Drout	drout	L dependence coefficient of the DIBL correction parameter in Rout	0.56	none	
Pscbe1	pscbe1	First substrate current body-effect parameter	4.24E8	V/m	
Pscbe2	pscbe2	Second substrate current body-effect parameter	1.0E-5	m/V	
Pvag	pvag	Gate dependence of Early voltage	0.0	none	
δ	delta	Effective Vds parameter	0.01	V	
Ngate	ngate	poly gate doping concentration	0	cm^{-3}	
$\alpha 0$	alpha0	The first parameter of impact ionization current	0	m/V	
$\beta 0$	beta0	The second parameter of impact ionization current	30	V	
Rsh	rsh	Source drain sheet resistance in ohm per square	0.0	Ω/ square	
Js0sw	jssw	Side wall saturation current density	0	A/m	
Jso	js	Source drain junction saturation current per unit area	1.E-4	A/ m^2	

A.3 AC and Capacitance Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Xpart	xpart	Charge partitioning rate flag	0	none	
CGS0	cgso	Non LDD region source-gate overlap capacitance per channel length	calculated	F/m	nC-1
CGD0	cgdo	Non LDD region drain-gate overlap capacitance per channel length	calculated	F/m	nC-2
CGB0	cgbo	Gate bulk overlap capacitance per unit channel length	0.0	F/m	
Cj	cj	Bottom junction per unit area	5e-4	F/m^2	
Mj	mj	Bottom junction capacitance grating coefficient	0.5		
Mjsw	mjsw	Source/Drain side junction capacitance grading coefficient	0.33	none	
Cjsw	cjsw	Source/Drain side junction capacitance per unit area	5.E-10	F/m	
Cjswg	cjswg	Source/drain gate sidwall junction capacitance grading coefficient	Cjsw	F/m	
Mjswg	mjswg	Source/drain gate sidewall junction capacitance coefficient	Mjsw	none	

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Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Pbsw	pbsw	Source/drain side junction built-in potential	1.0	V	
Pb	pb	Bottom built-in potential	1.0	V	
Pbswg	pbswg	Source/Drain gate sidewall junction built-in potential	Pbsw	V	
CGS1	cgs1	Light doped source-gate region overlap capacitance	0.0	F/m	
CGD1	cgd1	Light doped drain-gate region overlap capacitance	0.0	F/m	
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance Fringing field capacitance	0.6	F/m	
Cf	cf	fringing field capacitance	calculated	F/m	nC-3
CLC	clc	Constant term for the short channel model	0.1E-6	m	
CLE	cle	Exponential term for the short channel model	0.6	none	
DLC	dlc	Length offset fitting parame-ter from C-V	lint	m	
DWC	dwc	Width offset fitting parameter from C-V	wint	m	
Vfb	vfb	Flat-band voltage parameter (for capmod=0 only)	-1	V	

A.4 NQS Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Elm	elm	Elmore constant of the channel	5	none	

A.5 dW and dL Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Wl	wl	Coefficient of length dependence for width offset	0.0	m^{Wln}	
Wln	wln	Power of length dependence of width offset	1.0	none	
Ww	ww	Coefficient of width dependence for width offset	0.0	m^{Wwn}	
Wwn	wwn	Power of width dependence of width offset	1.0	none	
Wwl	wwl	Coefficient of length and width cross term for width offset	0.0	$m^{Wwn+Wln}$	
Ll	ll	Coefficient of length dependence for length offset	0.0	m^{Lln}	
Lln	lln	Power of length dependence for length offset	1.0	none	

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Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Lw	lw	Coefficient of width dependence for length offset	0.0	m^{Lwn}	
Lwn	lwn	Power of width dependence for length offset	1.0	none	
Lwl	lwl	Coefficient of length and width cross term for length offset	0.0	$m^{Lwn+Lln}$	

A.6 Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tnom	tnom	Temperature at which parameters are extracted	27	^{o}C	
μte	ute	Mobility temperature exponent	-1.5	none	
Kt1	kt1	Temperature coefficient for threshold voltage	-0.11	V	
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	0.0	V*m	
Kt2	kt2	Body-bias coefficient of Vth temperature effect	0.022	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Ua1	ua1	Temperature coefficient for Ua	4.31E-9	m/V	
Ub1	ub1	Temperature coefficient for Ub	-7.61E-18	$(m/V)^2$	
Uc1	uc1	Temperature coefficient for Uc	mob-mod=1, 2: -5.6E-11 mob-mod=3: -0.056	m/V^2 1/V	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
Prt	prt	Temperature coefficient for Rdsw	0	Ω-μm	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
nj	nj	Emission coefficient of junction	1	none	
XTI	xti	Junction current temperature exponent coefficient	3.0	none	

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A.7 Flicker Noise Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none	
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none	
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none	
Em	em	Saturation field	4.1e7	V/m	
Af	af	Frequency exponent	1	none	
Ef	ef	Flicker exponent	1	none	
Kf	kf	Flicker noise parameter	0	none	

A.8 Process Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tox	tox	Gate oxide thickness	1.5e-8	m	
Xj	xj	Junction Depth	1.5e-7	m	
$\gamma 1$	gamma1	Body-effect coefficient near the surface	calcu-lated	$V^{1/2}$	nI-4

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
$\gamma 2$	gamma2	Body-effect coefficient in the bulk	calcu-lated	$V^{1/2}$	nI-5
Nch	nch	Channel doping concentration	1.7e17	$1/cm^3$	nI-3
Nsub	nsub	Substrate doping concentration	6e16	$1/cm^3$	
Vbx	vbx	Vbs at which the depletion region width equals xt	calcu-lated	V	nI-6
Xt	xt	Doping depth	1.55e-7	m	

A.9 Bin Description Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Lmin	lmin	Minimum channel length	0.0	m	
Lmax	lmax	Maximum channel length	1.0	m	
Wmin	wmin	Minimum channel width	0.0	m	
Wmax	wmax	Maximum channel width	1.0	m	
binunit	binunit	Bin unit scale selector	1	none	

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A.10Model Parameter Notes

nI-1. If Vtho is not specified, it is calculated using:

$$V_{tho} = V_{FB} + \phi_s + K_1\sqrt{\phi_s}$$

where VFB=-1.0. If Vth0 is specified, VFB is calculated using

$$V_{FB} = V_{tho} - \phi_s - K_1\sqrt{\phi_s}$$

nI-2. If k1 and k2 are not given, they are calculated using:

$$K_1 = gamma_2 - 2K_2\sqrt{\phi_s - V_{bm}}$$

$$K_2 = \frac{(gamma1 - gamma2)(\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

where the parameter phi is calculated using:

$$\phi_s = 2v_{tm0}\,ln\left(\frac{Nch}{ni}\right)$$

$$v_{tm0} = \frac{k_B T_{nom}}{q}$$

$$n_i = 1.45x10^{10}\left(\frac{T_{nom}}{300.15}\right)^{1.5} exp\left(21.5565981 - \frac{E_{g0}}{2v_{tm0}}\right)$$

$$E_{g0} = 1.16 - \frac{7.02x10^{-4} T_{nom}^{2}}{T_{nom} + 1108}$$

where E_{g0} is the energy bandgap at temperature Tnom.

nI-3. If nch is not given and gamma1 is given, nch is calculated from:

$$N_{ch} = \frac{gamma1^2 C_{ox}^{2}}{2q\varepsilon_{si}}$$

If both gamma1 and nch are not given, nch defaults to 1.7e23 $1/m^3$ and gamma1 is calculated from nch.

nI-4. If gamma1 is not given, it is calculated using:

$$gamma_1 = \frac{\sqrt{2q\varepsilon_{si} N_{ch}}}{C_{ox}}$$

nI-5. If gamma2 is not given, it is calculated using:

$$gamma_2 = \frac{\sqrt{2q\varepsilon_{si} N_{sub}}}{C_{ox}}$$

nI-6. If vbx is not given, it is calculated using:

$$V_{bx} = \phi_s - \frac{qN_{ch}X_t^2}{2\varepsilon_{si}}$$

nC-1. If cgso is not given then it is calculated using:

if (dlc is given and is greater 0) then,

cgso = p1 = (dlc*cox) - cgs1

if (the previously calculated cgso <0), then

cgso=0

else cgso = 0.6 xj*cox

nC-2. If cgdo is not given then it is calculated using:

if (dlc is given and is greater than 0) then,

cgdo = p2 = (dlc*cox) - cgd1

if (the previously calculated cgdo <0), then

cgdo=0

else cgdo = 0.6 xj*cox

nC-3. If cf is not given then it is calculated using:

$$CF = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{4\times10^{-7}}{Tox}\right)$$

APPENDIX B: Equation List

B.1 I-V Model

B.1.1 Threshold Voltage

$$
\begin{aligned}
V_{th} = {} & V_{tho} + K_1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K_2 V_{bseff} \\
& + K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff})\frac{T_{OX}}{W_{eff}' + W_0}\Phi_s \\
& - D_{VT0w}\left(exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{2l_{tw}}) + 2exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{l_{tw}})\right)(V_{bi} - \Phi_s) \\
& - D_{VT0}\left(exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)(V_{bi} - \Phi_s) \\
& - \left(exp(-D_{sub}\frac{L_{eff}}{2l_{to}}) + 2exp(-D_{sub}\frac{L_{eff}}{l_{to}})\right)(E_{tao} + E_{tab}V_{bseff})\, V_{ds}
\end{aligned}
$$

$$
l_t = \sqrt{\varepsilon_{si} X_{dep} / C_{ox}}(1 + D_{VT2}V_{bseff})
$$

$$
l_{tw} = \sqrt{\varepsilon_{si} X_{dep} / C_{ox}}(1 + D_{VT2w}V_{bseff})
$$

$$
l_{to} = \sqrt{\varepsilon_{si} X_{dep0} / C_{ox}}
$$

$$
X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\Phi_s - V_{bseff})}{qN_{ch}}}
$$

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{si}\Phi_s}{qN_{ch}}}$$

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\ ] \qquad (\delta 1=0.001)$$

$$V_{bc} = 0.9(\phi s - \frac{K1^2}{4K2^2})$$

$$V_{bi} = v_t \ln(\frac{N_{ch}N_{DS}}{n_i^2})$$

B.1.2 Effective Vgs-Vth

$$V_{gsteff} = \frac{2\ n\ v_t \ln\left[1 + \exp(\frac{V_{gs} - V_{th}}{2\ n\ v_t})\right]}{1 + 2\ n\ \ C_{OX}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si}N_{ch}}}\exp(-\frac{V_{gs} - V_{th} - 2V_{off}}{2\ n\ v_t})}$$

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})\left(\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

$$C_d = \frac{\varepsilon_{si}}{X_{dep}}$$

B.1.3 Mobility

For Mobmod=1

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$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2}$$

For Mobmod=2

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff}}{T_{OX}}) + U_b(\frac{V_{gsteff}}{T_{OX}})^2}$$

For Mobmod=3

$$\mu_{eff} = \frac{\mu_o}{1 + [U_a(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2](1 + U_c V_{bseff})}$$

B.1.4 Drain Saturation Voltage

For Rds>0 or $\lambda \neq 1$:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{bulk}{}^2 W_{eff} \nu_{sat} C_{ox} R_{DS} + (\frac{1}{\lambda} - 1) A_{bulk}$$

$$b = -\left((V_{gsteff} + 2v_t)(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}(V_{gsteff} + 2v_t)W_{eff}v_{sat}C_{ox}R_{DS} \right)$$

$$c = (V_{gsteff} + 2v_t)E_{sat}L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff}v_{sat}C_{ox}R_{DS}$$

$$\lambda = A_1 V_{gsteff} + A_2$$

For Rds=0, λ=1:

$$V_{dsat} = \frac{E_{sat}\ L_{eff}\ (V_{gsteff} + 2v_t)}{A_{bulk}\ E_{sat}\ L_{eff} + (V_{gsteff} + 2v_t)}$$

$$A_{bulk} = (1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}[1 - A_{gs}V_{gsteff}(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}})^2] + \frac{B_o}{Weff' + B_1}\})\frac{1}{1 + K_{ETA}V_{bseff}}$$

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}$$

B.1.5 Effective Vds

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

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B.1.6 Drain Current Expression

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2v_t)}\right)V_{dseff}}{L_{eff}[1 + V_{dseff} / (E_{sat}L_{eff})]}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\ litl}(V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + P_{DIBLCB}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right)$$

$$\theta_{rout} = P_{DIBLC1}\left[\exp\left(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}\right) + 2\exp\left(-D_{ROUT}\frac{L_{eff}}{l_{t0}}\right)\right] + P_{DIBLC2}$$

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}\ litl}{V_{ds} - V_{dseff}}\right)$$

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{DS}v_{sat}C_{ox}W_{eff}V_{gsteff}[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)}]}{2/\lambda - 1 + R_{DS}v_{sat}C_{ox}W_{eff}A_{bulk}}$$

$$litl = \sqrt{\frac{\varepsilon_{si}T_{ox}X_j}{\varepsilon_{ox}}}$$

B.1.7 Substrate Current

$$I_{sub} = \frac{\alpha_o}{L_{eff}}(V_{ds} - V_{dseff})\exp(-\frac{\beta_o}{V_{ds} - V_{dseff}})\frac{I_{dso}}{1 + \frac{R_{ds}I_{dso}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

B.1.8 Polysilicon Depletion Effect

$$V_{poly} = \frac{1}{2}X_{poly}E_{poly} = \frac{qN_{gate}X_{poly}^2}{2\varepsilon_{si}}$$

$$\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_{poly} = \sqrt{2q\varepsilon_{si}N_{gate}V_{poly}}$$

$$V_{gs} - V_{FB} - \phi_s = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0$$

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$$a = \frac{\varepsilon_{ox}^2}{2q\varepsilon_{si}N_{gate}T_{ox}^2}$$

$$V_{gs\_eff} = V_{FB} + \phi_s + \frac{q\varepsilon_{si}N_{gate}T_{ox}^2}{\varepsilon_{ox}^2}\left(\sqrt{1+\frac{2\varepsilon_{ox}^2(V_{gs}-V_{FB}-\phi_s)}{q\varepsilon_{si}N_{gate}T_{ox}^2}}-1\right)$$

B.1.9 Effective Channel Length and Width

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W_{eff}' = W_{drawn} - 2dW'$$

$$dW = dW' + dW_g V_{gsteff} + dW_b\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right)$$

$$dW' = W_{\text{int}} + \frac{W_l}{L^{W\ln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{W\ln}W^{Wwn}}$$

$$dL = L_{\text{int}} + \frac{L_l}{L^{L\ln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{L\ln}W^{Lwn}}$$

B.1.10Drain/Source Resistance

$$R_{ds} = \frac{R_{dsw}[1 + \mathrm{P_r}_{wg} V_{gsteff} + \mathrm{P_r}_{wb}(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})]}{(10^6 W_{eff}')^{Wr}}$$

B.1.11Temperature Effects

$$V_{th(T)} = V_{th(Tnorm)} + (K_{T1} + K_{t1l} / L_{eff} + K_{T2} V_{bseff})(T / T_{norm} - 1)$$

$$\mu_{o(T)} = \mu_{o(Tnorm)} (\frac{T}{T_{norm}})^{\mu_{te}}$$

$$v_{sat(T)} = v_{sat(Tnorm)} - A_T(T / T_{norm} - 1)$$

$$R_{dsw(T)} = R_{dsw(Tnorm)} + \mathrm{P_r}_t(\frac{T}{T_{norm}} - 1)$$

$$U_{a(T)} = U_{a(Tnorm)} + U_{a1}(T / T_{norm} - 1)$$

$$U_{b(T)} = U_{b(Tnorm)} + U_{b1}(T / T_{norm} - 1)$$

$$U_{c(T)} = U_{c(Tnorm)} + U_{c1}(T / T_{norm} - 1)$$

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B.2 Capacitance Model Equations

B.2.1 Dimension Dependence

$$\delta W_{eff} = DWC + \frac{Wl}{L^{Wln}} + \frac{Ww}{W^{Wwn}} + \frac{Wwl}{L^{Wln}W^{Wwn}}$$

$$\delta L_{eff} = DLC + \frac{Ll}{L^{Lln}} + \frac{Lw}{W^{Lwn}} + \frac{Lwl}{L^{Lln}W^{Lwn}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

B.2.2 Overlap Capacitance (for NMOS)

B.2.2.1 Source Overlap Capacitance

(1) for capmod=0

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0V_{gs}$$

(2) for capmod=1

if (Vgs <0)

$$\frac{Q_{overlap,s}}{W_{active}} = \mathrm{CGS0}V_{gs} + \frac{\mathrm{CKAPPA}\,\mathrm{CGS1}}{2}\left(-1+\sqrt{1-\frac{4V_{gs}}{\mathrm{CKAPPA}}}\right)$$

else

$$\frac{Q_{overlap,s}}{W_{active}} = (\mathrm{CGS0} + \mathrm{CKAPPA}\,\mathrm{CGS1})\,\mathrm{Vgs}$$

(3) for capmod=2

$$V_{gs,overlap} = \frac{1}{2}\left\{\left(V_{gs}-\delta_1\right)+\sqrt{\left(V_{gs}-\delta_1\right)^2-4\delta_1}\right\} \quad where \quad \delta_1 = 0.02$$

$$\frac{Q_{overlap,s}}{W_{active}} = \mathrm{CGS0}V_{gs} + \mathrm{CGS1}\left\{V_{gs} - V_{gs,overlap} + \frac{\mathrm{CKAPPA}}{2}\left(-1+\sqrt{1+\frac{4V_{gs,overlap}}{\mathrm{CKAPPA}}}\right)\right\}$$

B.2.2.2 Drain Overlap Capacitance

(1) for capmod=0

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$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd}$$

(2) for capmod=1

if (Vgd <0)

$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd} + \frac{\text{CKAPPACGD1}}{2}\left(-1+\sqrt{1-\frac{4V_{gd}}{\text{CKAPPA}}}\right)$$

else

$$\frac{Q_{overlap,d}}{W_{active}} = (\text{CGD0} + \text{CKAPPACGD1})\,\text{Vgd}$$

(3) for capmod=2

$$V_{gd,overlap} = \frac{1}{2}\left\{\left(V_{gd}-\delta_2\right)+\sqrt{\left(V_{gd}-\delta_2\right)^2-4\delta_2}\right\} \quad where \quad \delta_2 = 0.02$$

$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd} + \text{CGD1}\left\{V_{gd} - V_{gd,overlap} + \frac{\text{CKAPPA}}{2}\left(-1+\sqrt{1+\frac{4V_{gd,overlap}}{\text{CKAPPA}}}\right)\right\}$$

B.2.2.3 Gate Overlap Charge

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right)$$

B.2.3 Instrinsic Charges

(1) for capmod=0

a) Accumulation region (Vgs <Vfb+Vbs)

$$Q_g = W_{active} L_{active} C_{ox} \left(V_{gs} - V_{bs} - V_{fb}\right)$$

$$Q_{sub} = -Q_g$$

$$Q_{inv} = 0$$

b) Subthreshold region (Vgs <Vth)

$$Q_b = -W_{active} L_{active} C_{ox} \frac{K_1^{\,2}}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{fb} - V_{bs}\right)}{K_1^{\,2}}}\right)$$

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$$Q_g = -Q_b$$

$$Q_{inv} = 0$$

c) Strong inversion (Vgs>Vth)

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}'}$$

$$A_{bulk}' = A_{bulk0}\left(1 + \left(\frac{\mathrm{CLC}}{L_{eff}}\right)^{\mathrm{CLE}}\right)$$

$$A_{bulk0} = \left(1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bs}}}\left\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} + \frac{B_o}{W_{eff}' + B_1}\right\}\right)\frac{1}{1 + K_{ETA} V_{bs}}$$

$$V_{th} = V_{fb} + \Phi_s + K_1\sqrt{\Phi_s - V_{bsf}}$$

(i) 50/50 Charge partition

if Vds<Vdsat

$$Q_g = C_{ox} W_{active} L_{active} [V_{gs} - V_{fb} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2})}]$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_s = Q_d = 0.5 Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - \Phi_s - \frac{V_{dsat}}{3})$$

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$$Q_s = Q_d = -\frac{1}{3} W_{active} L_{active} C_{ox} (V_{gs} - V_{th})$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3})$$

(ii) 40/60 channel-charge Partition

if (Vds <Vdsat)

$$Q_g = C_{ox} W_{active} L_{active} [V_{gs} - V_{fb} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2})}]$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}')V_{ds}}{2} - \frac{(1 - A_{bulk}')A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_d = -W_{active} L_{active} C_{ox}$$
$$\left[\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}'}{2} V_{ds} + \frac{A_{bulk}' V_{ds} [\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{(A_{bulk}' V_{ds})^2}{40}}{(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})^2} \right]$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - \Phi_s - \frac{V_{dsat}}{3})$$

$$Q_d = -\frac{4}{15} W_{active} L_{active} C_{ox} (V_{gs} - V_{th})$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}') V_{dsat}}{3})$$

(iii) 0/100 Channel-charge Partition

if Vds <Vdsat

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$$Q_g = C_{ox} W_{active} L_{active} [V_{gs} - V_{fb} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2})}]$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_d = -W_{active} L_{active} C_{ox} \left[\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}'}{4} V_{ds} - \frac{(A_{bulk}' V_{ds})^2}{24(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})} \right]$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - \Phi_s - \frac{V_{dsat}}{3})$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3})$$

$$Q_d = 0$$

$$Q_s = -(Q_g + Q_b)$$

(2) for capmod=1

if (Vgs <Vfb+Vbs+Vgsteffcv)

$$Q_{g1} = -W_{active} L_{active} C_{ox} \left(V_{gs} - Vfb \ - V_{bs} - V_{gsteffcv} \right)$$

else

$$Q_{g1} = W_{active} L_{active} C_{ox} \frac{\mathrm{K}_1{}^2}{2} \left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FB} - V_{gsteff} cv - V_{bs} \right)}{\mathrm{K}_1{}^2}} \right)$$

$$Q_{b1} = -Q_{g1}$$

$$V_{dsat,cv} = \frac{V_{gsteffcv}}{A_{bulk}'}$$

$$\mathrm{A_{bulk}'} = \mathrm{A_{bulk0}}\left(1+\left(\frac{CLC}{\mathrm{L_{eff}}}\right)^{CLE}\right)$$

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_o}{W_{eff}'+B_1}\}\right)\frac{1}{1+K_{ETA}V_{bseff}}$$

$$V_{gsteffcv} = n\,v_t \ln\left[1+\exp(\frac{V_{gs}-V_{th}}{n\,v_t})\right]$$

if (Vds <=Vdsat)

$$Q_g = Q_{g1} + W_{active}L_{active}C_{ox}\left(V_{gsteff\,cv} - \frac{V_{ds}}{2} + \frac{A_{bulk}'V_{ds}^{\,2}}{12\left(V_{gsteff\,cv}-\frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

$$Q_b = Q_{b1} + W_{active}L_{active}C_{ox}\left(\frac{1-A_{bulk}'}{2}V_{ds} - \frac{(1-A_{bulk}')A_{bulk}'V_{ds}^{\,2}}{12\left(V_{gsteffcv}-\frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

(i) 50/50 Channel-charge Partition

$$Q_s = Q_d = -\frac{W_{active} L_{active} C_{ox}}{2}\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2} V_{ds} + \frac{A_{bulk}'^2 V_{ds}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right)$$

(ii) 40/60 Channel-charge partition

$$Q_s = -\frac{W_{active} L_{active} C_{ox}}{2\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2} V_{ds} \right)^2}$$
$$\left(V_{gsteffcv}^3 - \frac{4}{3} V_{gstefcvf}^2 \left(A_{bulk}' V_{ds} \right) + \frac{2}{3} V_{gsteffcv} \left(A_{bulk}' V_{ds} \right)^2 - \frac{2}{15} \left(A_{bulk}' V_{ds} \right)^3 \right)$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(iii) 0/100 Channel-charge Partition

$$Q_s = -W_{active} L_{active} C_{ox}\left(\frac{V_{gstefcv}}{2} + \frac{A_{bulk}' V_{ds}}{4} - \frac{\left(A_{bulk}' V_{ds} \right)^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right)$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

if (Vds >Vdsat)

$$Q_g = Q_{g1} + W_{active} L_{active} C_{ox} \left(V_{gsteff\,cv} - \frac{V_{dsat}}{3} \right)$$

$$Q_b = Q_{b1} - W_{active} L_{active} C_{ox} \frac{\left(V_{gsteffcv} - V_{dsat} \right)}{3}$$

(i) 50/50 Channel-charge Partition

$$Q_s = Q_d = -\frac{W_{active} L_{active} C_{ox}}{3} V_{gsteff\,cv}$$

(ii) 40/60 Channel-charge Partition

$$Q_s = -\frac{2W_{active} L_{active} C_{ox}}{5} V_{gsteffcv}$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(iii) 0/100 Channel-charge Partition

$$Q_s = -W_{active} L_{active} C_{ox} \frac{2V_{gstefcv}}{3}$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(3) for capmod=2

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub}\right)$$

$$Q_b = Q_{acc} + Q_{sub0} + \delta Q_{sub}$$

$$Q_{inv} = Q_s + Q_d$$

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3{}^2 + 4\delta_3 vfb}\right\} \quad where \quad V_3 = vfb - V_{gb} - \delta_3; \quad \delta_3 = 0.02$$

$$vfb = V_{th} - \phi_s - K_1\sqrt{\phi_s}$$

$$Q_{acc} = -W_{active} L_{active} C_{ox}\left(V_{FBeff} - vfb\right)$$

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1{}^2}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FBeff} - V_{gsteff\,cv} - V_{bseff}\right)}{K_1{}^2}}\right)$$

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}'}$$

$$A_{bulk}' = A_{bulk0}\left(1+\left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right.$$

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_o}{W_{eff}'+B_1}\}\right)\frac{1}{1+K_{ETA}V_{bseff}}$$

$$V_{gsteffcv} = n\,v_t \ln\left[1+\exp(\frac{V_{gs}-V_{th}}{n\,v_t})\right]$$

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^{\,2}+4\delta_4 V_{dsat,cv}}\right\} \quad where \quad V_4 = V_{dsat,cv} - V_{ds} - \delta_4; \quad \delta_4 = 0.02$$

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left(\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)+\frac{A_{bulk}'^{\,2}V_{cveff}^{\,2}}{12\left(V_{gsteff\,cv}-\frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

$$\delta Q_{sub} = W_{active}L_{active}C_{ox}\left(\frac{1-A_{bulk}'}{2}V_{cveff} - \frac{(1-A_{bulk}')A_{bulk}'V_{cveff}^{\,2}}{12\left(V_{gsteffcv}-\frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

B.2.3.1 50/50 Charge partition

$$Q_s = Q_d = 0.5Q_{inv} = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2}V_{cveff} + \frac{A_{bulk}'^{\,2}\,V_{cveff}^{\,2}}{12\left(V_{gsteffcv} - \frac{A_{bulk}}{2}V_{cveff}\right)}\right)$$

B.2.3.2 40/60 Channel-charge Partition

$$Q_s = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^{\,3} - \frac{4}{3}V_{gsteffcv}^{\,2}\left(A_{bulk}'V_{cveff}\right) + \frac{2}{3}V_{gsteff}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

$$Q_d = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^{\,3} - \frac{5}{3}V_{gsteffcv}^{\,2}\left(A_{bulk}'V_{cveff}\right) + V_{gsteff\,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

B.2.3.3 0/100 Charge Partition

$$Q_s = -W_{active}L_{active}C_{ox}\left(\frac{V_{gsteffcv}}{2} + \frac{A_{bulk}'V_{cveff}}{4} - \frac{\left(A_{bulk}'V_{cveff}\right)^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

$$Q_d = -W_{active}L_{active}C_{ox}\left(\frac{V_{gsteffcv}}{2} - \frac{3A_{bulk}'V_{cveff}}{4} + \frac{\left(A_{bulk}'V_{cveff}\right)^2}{8\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

B.2.4 Intrinsic Capacitances (with Body bias and DIBL)

$$C_{(s,d,g,b),g} = \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}}$$

$$C_{(s,d,g,b),s} = -\frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} + \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \left(\frac{\partial V_{th}}{\partial V_{ds}} + \frac{\partial V_{th}}{\partial V_{bs}} \right)$$

$$C_{(s,d,g,b),d} = \frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}cv} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{ds}}$$

$$C_{(s,d,g,b),b} = \frac{\partial Q_{s,d,g,b}}{\partial V_{bs}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}{}^{cv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{bs}}$$

B.3 NQS Model Equations:

Quasi-static equilibrium channel charge:

$$Q_{eq} = -(Q_g + Q_b)$$

Actual channel charge and *Qdef* obtained from subcircuit (Figure 5-2):

$$Q_{ch} = Q_{eq} - Q_{def}$$

$$g_\tau = \frac{1}{\tau} = \frac{1}{\tau_{drift}} + \frac{1}{\tau_{diff}}$$

$$\tau_{drift} = \frac{C_{ox} W_{eff} {L_{eff}}^3}{\mu_{eff} \varepsilon \left| Q_{eq} - \alpha Q_{def} \right|} \approx \frac{\zeta}{\left| Q_{eq} \right|}$$

where,

$\varepsilon \equiv$ Elmore Constant $(default = 5)$ $0.0 \le \alpha \le 1.0$ $(default = 0.5)$

and

$$\zeta = \frac{C_{ox} W_{eff} {L_{eff}}^3}{\mu_{eff} \varepsilon}$$

$$\tau_{diff} = \frac{q {L_{eff}}^2}{16 \mu_{eff} KT}$$

B.4 Flicker Noise

There exists two models for flicker noise. Each of these can be toggled by the **noimod** flag.

1. For noimod=1 and 4

$$Flic\ker Noise = \frac{K_f {I_{ds}}^{af}}{C_{ox} {L_{eff}}^2 f^{ef}}$$

2. For noimod=2 and 3
   1. Vgs>Vth+0.1:

$$Flic\ker Noise = \frac{vtq^2 I_{ds} \mu_{eff}}{f^{Ef} {L_{eff}}^2 C_{ox} 10^8} [N_{oia} \log(\frac{No + 2x10^{14}}{Nl + 2x10^{14}}) + N_{oib}(No - Nl)$$

$$+0.5 N_{oic}(No^2 - Nl^2)] + \frac{vt {I_{ds}}^2 \Delta L_{clm}}{f^{Ef} {L_{eff}}^2 W_{eff} 10^8} \frac{N_{oia} + N_{oib} Nl + N_{oic} Nl^2}{(Nl + 2x10^{14})^2}$$

where V_{tm} is the thermal voltage, μ_{eff} is the effective mobiity at the given bias condition, L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source given by:

$$N_0 = \frac{C_{ox}(V_{GS} - V_{TH})}{q}$$

The parameter N_l is the charge density at the drain given by:

$$N_l = \frac{C_{ox}(V_{GS} - V_{TH} - V_{DS}')}{q}$$

$$V_{DS}' = MIN(V_{DS}, V_{DSAT})$$

ΔLclm refers to channel length reduction due to CLM and is given by:

$$\Delta L_{clm} = \begin{cases} Litl \times \log\left(\frac{\frac{V_{DS} - V_{DSAT}}{Litl} + Em}{E_{SAT}}\right) & \text{if VDS > VDSAT} \\ 0 & \text{otherwise} \end{cases}$$

$$E_{SAT} = \frac{2 \times Vsat}{u_{eff}}$$

2. Otherwise,

$$FlickerNoise = \frac{S_{limit} \times S_{wi}}{S_{limit} + S_{wi}}$$

Where, S_{limit} is the flicker noise calculated at Vgs=Vth+0.1 and S_{wi} is given by:

$$Swi = \frac{Noia\,Vt\,Ids^{2}}{Weff\,Leff \quad f^{Ef}\,4x10^{36}}$$

B.5 Channel Thermal Noise

There exists two models for channel thermal noise. Each of these can be toggled by the **noimod** flag.

1. For noimod=1 and 3

$$\frac{8kT}{3}(gm + gds + gmb)$$

2. For noimod=2 and 4

$$\frac{4KT\mu_{eff}}{Leff^{2}}|Q_{inv}|$$

$$Q_{inv} = -W_{eff} L_{eff} C_{ox} V_{gsteff} (1 - \frac{A_{bulk}}{2(V_{gsteff} + 2vt)} V_{dseff})$$

The derivation for this last thermal noise expression is based on the noise model found in [35].

APPENDIX C: References

[1] G.S. Gildenblat, **VLSI Electronics: Microstructure Scienc**e, p.11, vol. 18, 1989.

[2] Muller and Kamins, **Devices Electronics for Integrated Circuits**, Second Edition.

[3] J. H. Huang, Z. H. Liu, M. C. Jeng, K. Hui, M. Chan, P. K. Ko and C. Hu., BSIM3 Version 2.0 User's Manual, March 1994.

[4] J.A. Greenfield and R.W. Dutton, "Nonplanar VLSI Device Analysis Using the Solution of Poisson's Equation," *IEEE Trans. Electron Devices*, vol. ED-27, p.1520, 1980.

[5] H.S. Lee. "An Analysis of the Threshold Voltage for Short-Channel IGFET's," *Solid-State Electronics*, vol.16, p.1407, 1973.

[6] G.W. Taylor, "Subthreshold Conduction in MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-25, p.337, 1978.

[7] T. Toyabe and S. Asai, "Analytical Models of Threshold Voltage and Breakdown Voltage of Short-Channel MOSFET's Derived from Two-Dimensional Analysis," *IEEE J. Solid-State Circuits*, vol. SC-14, p.375, 1979.

[8] D.R. Poole and D.L. Kwong, "Two-Dimensional Analysis Modeling of Threshold Voltage of Short-Channel MOSFET's," *IEEE Electron Device Letter*, vol. ED-5, p.443, 1984.

[9] J.D. Kendall and A.R. Boothroyd, "A Two-Dimensional Analytical Threshold Voltage Model for MOSFET's with Arbitrarily Doped Substrate," *IEEE Electron Device Letter*, vol. EDL-7, p.407, 1986.

[10] Z.H. Liu, C. Hu, J.H. Huang, T.Y. Chan, M.C. Jeng, P.K. Ko, and Y.C. Cheng, "Threshold Voltage Model For Deep-Submicrometer MOSFETs," *IEEE Tran. Electron Devices*, vol. 40, pp. 86-95, Jan., 1993.

[11] Y.C. Cheng and E.A. Sullivan, "Effect of Coulombic Scattering on Silicon Surface Mobility," *J. Appl. Phys.* 45, 187 (1974).

[12] Y.C. Cheng and E.A. Sullivan, *Surf. Sci*. 34, 717 (1973).

[13] A.G. Sabnis and J.T. Clemens, "Characterization of Electron Velocity in the Inverted <100> Si Surface," *Tech. Dig.- Int. Electron Devices Meet.*, pp. 18-21 (1979).

[14] G.S. Gildenblat, **VLSI Electronics: Microstructure Science**, p. 11, vol. 18, 1989.

[15] M.S. Liang, J.Y. Choi, P.K. Ko, and C. Hu, "Inversion-Layer Capacitance and Mobility of Very Thin Gate-Oxide MOSFET's," *IEEE Trans. Electron Devices*, ED-33, 409, 1986.

[16] F. Fang and X. Fowler, "Hot-electron Effects and Saturation velocity in Silicon Inversion Layer," *J. Appl. Phys.*, 41, 1825, 1969.

[17] E. A. Talkhan, I. R. Manour and A. I. Barboor, "Investigation of the Effect of Drift-Field-Dependent Mobility on MOSFET Characteristics," Parts I and II. *IEEE Trans. on Electron Devices*, ED-19(8), 899-916, 1972.

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[18] M.C. Jeng, "Design and Modeling of Deep-Submicrometer MOSFETs," Ph. D. Dissertation, University of California.

[19] K.Y. Toh, P.K. Ko and R.G. Meyer, "An Engineering Model for Short-channel MOS Devices," *IEEE Jour. of Solid-State Circuits*, vol. 23, No. 4, Aug. 1988.

[20] C. Hu, S. Tam, F.C. Hsu, P.K. Ko, T.Y. Chan and K.W. Kyle, "Hot-Electron Induced MOSFET Degradation - Model, Monitor, Improvement," *IEEE Tran. on Electron Devices*, Vol. 32, pp. 375-385, Feb. 1985.

[21] F.C. Hsu, P.K. Ko, S. Tam, C. Hu and R.S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," *IEEE Trans. on Electron Devices*, Vol.ED-29, pp. 1735, Nov. 1982

[22] H. J. Parke, P. K. Ko, and C. Hu, " A Measurement-based Charge Sheet Capacitance Model of Short-Channel MOSFET's for SPICE," in *IEEE IEDM 86, Tech. Dig.*, pp. 485-488, Dec. 1986.

[23] M. Shur, T.A. Fjeldly, T. Ytterdal, and K. Lee, " A Unified MOSFET Model," *Solid-State Electron.*, 35, pp. 1795-1802, 1992.

[24] MOS9 Documentation.

[25] C. F. Machala, P. C. Pattnaik and P. Yang, "An Efficient Algorithms for the Extraction of Parameters with High Confidence from Nonlinear Models," *IEEE Electron Device Letters*, Vol. EDL-7, no. 4, pp. 214-218, 1986.

[26] Y. Tsividis and K. Suyama, "MOSFET Modeling for Analog Circuit CAD: Problems and Prospects," *Tech. Dig.* vol. CICC-93, pp. 14.1.1-14.1.6, 1993.

[27] C. L. Huang and G. Sh. Gildenblat, "Measurements and Modeling of the n-channel MOSFET Inversion Layer Mobility and Device Characteristics in the Temperature Range 60-300 K," *IEEE Tran. on Electron Devices*, vol. ED-37, no.5, pp. 1289-1300, 1990.

[28] D. S. Jeon, et al, *IEEE Tran. on Electron Devices*, vol. ED-36, no. 8, pp1456-1463, 1989.

[29] S. M. Sze, **Physics of Semiconductor Devices**, 2nd Edition.

[30] P. Gray and R. Meyer, **Analysis and Design of Analog Integrated Circuits**, Second Edition.

[31] Mansun Chan, et al, "A Relaxation time Approach to Model the Non-Quasi-Static Transient Effects in MOSFETs," IEDM, 1994 Technical Digest, pp. 169-172, Dec. 1994.

[32] P. K. Ko, “Hot-electron Effects in MOSFET’s”, Ph. D Dissertation, University of California, Berkeley, 1982

[33] K.K. Hung et al, “A Physics-Based MOSFET Noise Model for Circuit Simulators,” IEEE Transactions on Electron Devices, vol. 37, no. 5, May 1990.

[34] K.K. Hung et al, “A Unified Model for the Flicker Noise in Metal-Oxide Semiconductor Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 37, no. 3, March 1990.

[35] T.P. Tsividis, **Operation and Modeling of the MOS Transistor**, McGraw-Hill, New York, 1987.

APPENDIX D: Binning BSIM3v3 Parameters

Below is a list of all BSIM3v3 model parameters which can or cannot be binned. All model parameters which can be binned follow the following implementation:

$$P = P_0 + \frac{P_L}{L_{eff}} + \frac{P_W}{W_{eff}} + \frac{P_p}{L_{eff} \times W_{eff}}$$

For example, for the parameter k1: P_0=k1, P_L=lk1, P_W=wk1, P_P=pk1. Binunit is a bin unit selector. If binunit=1, the units of Leff and Weff used in the binning equation above have the units of microns. Otherwise, they are in meters.

For example, for a device with Leff=0.5μm and Weff=10μm. If binunit = 1, the parameter values for vsat are 1e5, 1e4, 2e4, and 3e4 for vsat, lvsat, wvsat, and pvsat, respectively. Therefore, the effective value of vsat for this device is:

vsat = 1e5 + 1e4/0.5 + 2e4/10 + 3e4/(0.5*10) = 1.28e5

To get the same effective value of vsat for binunit = 0, the values of vsat, lvsat, wvsat, and pvsat would be 1e5, 1e-2, 2e-2, 3e-8, respectively. Thus,

vsat = 1e5 + 1e-2/0.5e6 + 2e-2/10e-6 + 3e-8/(0.5e-6 * 10e-6) = 1.28e5

As a final note: although BSIM3v3 supports binning as an option for model extraction, it is not strongly recommended.

D.1 BSIM3v3 Model Control Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
none	level	BSIMv3 model selector	NO
Mobmod	mobmod	Mobility model selector	NO
Capmod	capmod	Flag for the short channel capacitance model	NO
Nqsmod	nqsmod	Flag for NQS model	NO
Noimod	noimod	Flag for Noise model	NO

D.2 DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Vth0	vth0	Threshold voltage @Vbs=0 for Large L.	YES
K1	k1	First order body effect coefficient	YES
K2	k2	Second order body effect coefficient	YES
K3	k3	Narrow width coefficient	YES
K3b	k3b	Body effect coefficient of k3	YES
W0	w0	Narrow width parameter	YES
Nlx	nlx	Lateral non-uniform doping parameter	YES

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Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Dvt0	dvt0	first coefficient of short-channel effect on Vth	YES
Dvt1	dvt1	Second coefficient of short-channel effect on Vth	YES
Dvt2	dvt2	Body-bias coefficient of short-channel effect on Vth	YES
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	YES
Dvt1w	dvtw1	Second coefficient of narrow width effect on Vth for small channel length	YES
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	YES
μ0	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	YES
Ua	ua	First-order mobility degradation coefficient	YES
Ub	ub	Second-order mobility degradation coefficient	YES
Uc	uc	Body-effect of mobility degradation coefficient	YES
νsat	vsat	Saturation velocity at Temp = Tnom	YES
A0	a0	Bulk charge effect coefficient for channel length	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Ags	ags	gate bias coefficient of Abulk	YES
B0	b0	Bulk charge effect coefficient for channel width	YES
B1	b1	Bulk charge effect width offset	YES
Keta	keta	Body-bias coefficient of bulk charge effect	YES
A1	a1	First non0saturation effect parameter	YES
A2	a2	Second non-saturation factor	YES
Rdsw	rdsw	Parasitic resistance per unit width	YES
Prwb	prwb	Body effect coefficient of Rdsw	YES
Prwg	prwg	Gate bias effect coefficient of Rdsw	YES
Wr	wr	Width Offset from Weff for Rds calculation	YES
Wint	wint	Width offset fitting parameter from I-V without bias	NO
Lint	lint	Length offset fitting parameter from I-V without bias	NO
dWg	dwg	Coefficient of Weff's gate dependence	YES
dWb	dwb	Coefficient of Weff's substrate body bias dependence	YES
Voff	voff	Offset voltage in the subthresh-old region for large W and L	Yes
Nfactor	nfactor	Subthreshold swing factor	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Eta0	eta0	DIBL coefficient in subthreshold region	YES
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect	YES
Dsub	dsub	DIBL coefficient exponent in subthreshold region	YES
Cit	cit	Interface trap capacitance	YES
Cdsc	cdsc	Drain/Source to channel coupling capacitance	YES
Cdscb	cdscb	Body-bias sensitivity of Cdsc	YES
Cdscd	cdscd	Drain-bias sensitivity of Cdsc	YES
Pclm	pclm	Channel length modulation parameter	YES
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	YES
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	YES
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	YES
Drout	drout	L dependence coefficient of the DIBL correction parameter in Rout	YES
Pscbe1	pscbe1	First substrate current body-effect parameter	YES
Pscbe2	pscbe2	Second substrate current body-effect parameter	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Pvag	pvag	Gate dependence of Early voltage	YES
δ	delta	Effective Vds parameter	YES
Ngate	ngate	poly gate doping concentration	YES
$\alpha 0$	alpha0	The first parameter of impact ionization current	YES
$\beta 0$	beta0	The second parameter of impact ionization current	YES
Rsh	rsh	Source drain sheet resistance in ohm per square	NO
Jso	js	Source drain junction saturation current per unit area	NO

D.3 AC and Capacitance Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Xpart	xpart	Charge partitioning rate flag	NO
CGS0	cgso	Non LDD region source-gate overlap capacitance per channel length	NO

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
CGD0	cgdo	Non LDD region drain-gate overlap capacitance per channel length	NO
CGB0	cgbo	Gate bulk overlap capacitance per unit channel length	NO
Cj	cj	Bottom junction per unit area	NO
Mj	mj	Bottom junction capacitance grating coefficient	NO
Mjsw	mjsw	Source/Drain side junction capacitance grading coeffi-cient	NO
Cjsw	cjsw	Source/Drain side junction capacitance per unit area	NO
Pb	pb	Bottom built-in potential	NO
Pbsw	pbsw	Source/Drain side junction built-in potential	NO
CGS1	cgs1	Light doped source-gate region overlap capacitance	YES
CGD1	cgd1	Light doped drain-gate region overlap capacitance	YES
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance Fringing field capacitance	YES
Cf	cf	fringing field capacitance	YES
CLC	clc	Constant term for the short channel model	YES
CLE	cle	Exponential term for the short channel model	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
DLC	dlc	Length offset fitting parameter from C-V	YES
DWC	dwc	Width offset fitting parameter from C-V	YES
Vfb	vfb	Flat-band voltage parameter (for capmod=0 only)	YES

D.4 NQS Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Elm	elm	Elmore constant of the channel	YES

D.5 dW and dL Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Wl	wl	Coefficient of length dependence for width offset	NO
Wln	wln	Power of length dependence of width offset	NO
Ww	ww	Coefficient of width dependence for width offset	NO
Wwn	wwn	Power of width dependence of width offset	NO
Wwl	wwl	Coefficient of length and width cross term for width offset	NO
Ll	ll	Coefficient of length dependence for length offset	NO
Lln	lln	Power of length dependence for length offset	NO
Lw	lw	Coefficient of width dependence for length offset	NO
Lwn	lwn	Power of width dependence for length offset	NO
Lwl	lwl	Coefficient of length and width cross term for length offset	NO

D.6 Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Tnom	tnom	Temperature at which parameters are extracted	NO
μte	ute	Mobility temperature exponent	YES
Kt1	kt1	Temperature coefficient for threshold voltage	YES
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	YES
Kt2	kt2	Body-bias coefficient of Vth temperature effect	YES
Ua1	ua1	Temperature coefficient for Ua	YES
Ub1	ub1	Temperature coefficient for Ub	YES
Uc1	uc1	Temperature coefficient for Uc	YES
At	at	Temperature coefficient for saturation velocity	YES
Prt	prt	Temperature coefficient for Rdsw	YES
nj	nj	Emission coefficient	YES
XTI	xti	Junction current temperature exponent coefficient	YES

D.7 Flicker Noise Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Noia	noia	Noise parameter A	NO
Noib	noib	Noise parameter B	NO
Noic	noic	Noise parameter C	NO
Em	em	Saturation field	NO
Af	af	Frequency exponent	NO
Ef	ef	Frequency exponent	NO
Kf	kf	Flicker noise parameter	NO

D.8 Process Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Tox	tox	Gate oxide thickness	NO
Xj	xj	Junction Depth	YES
$\gamma 1$	gamma1	Body-effect coefficient near the surface	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
$\gamma 2$	gamma2	Body-effect coefficient in the bulk	YES
Nch	nch	Channel doping concentration	YES
Nsub	nsub	Substrate doping concentration	YES
Vbx	vbx	Vbs at which the depletion region width equals xt	YES
Vbm	vbm	Maximum applied body bias in Vth calculation	YES
Xt	xt	Doping depth	YES

D.9 Bin Description Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Lmin	lmin	Minimum channel length	NO
Lmax	lmax	Maximum channel length	NO
Wmin	wmin	Minimum channel width	NO
Wmax	wmax	Maximum channel width	NO
binunit	binunit	Bin unit selector	NO