
Low-power design techniques and CAD tools for analog and RF integrated circuits

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1 PRACTICAL HARMONIC OSCILLATOR DESIGN

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An oscillator is what you get when you try to build an amplifier. This is a popular definition of an oscillator. There is some truth in this statement. Surely, it takes a good amplifier circuit to create an oscillator. It also takes a good resonator to build a harmonic oscillator. On-chip passive components have evolved considerably the last few years. Flip-chip techniques have enabled high Q on-board resonators.

Meanwhile supply voltage of communications equipment is decreasing whereas phase noise requirements are becoming more and more severe. The design of an oscillator for telecommunication applications still constitutes a major challenge for the electronic designer. This chapter proposes a well-structured way to oscillator design by giving both theoretical considerations and practical oscillator implementation examples.

1.1 INTRODUCTION

An oscillator is an active electrical circuit that can generate periodic waveforms out of constants [1]. This short definition is illustrated in Figure 12.1.

DC energy from the power supply is transformed into the time varying oscillator output signal

$$A(t) = \hat{A} \Psi(\omega_0 t + \theta) \quad (1.1)$$

characterized by the following parameters

- Waveform Ψ
- Amplitude \hat{A}
- Frequency ω_0

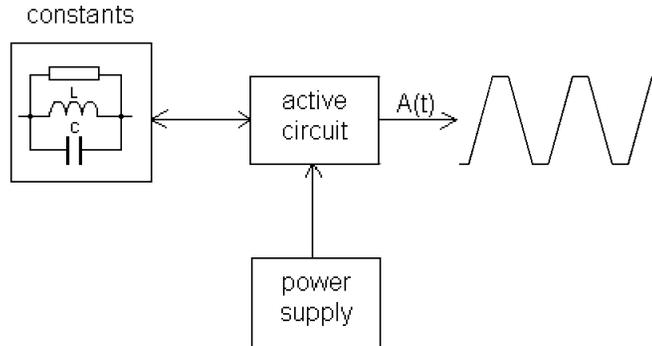


Figure 1.1 Figure 12.1: An oscillator generates a periodic waveform out of constants

In an ideal oscillator circuit, the oscillation frequency ω_0 depends only on the constants and not on the active part. In a practical oscillator circuit, the active part does have an influence the oscillation frequency. Part of the frequency determining constants may be constituted by the active circuit's parasitic capacitances.

The oscillator can be more precisely characterized by its frequency accuracy and both long and short-term stability. Especially the short-term frequency fluctuations, often referred to as phase noise have become a driving factor for the oscillator circuits used in today's communication equipment. Low noise oscillators use frequency selective devices or resonators to determine the oscillation frequency.

1.2 THE HARMONIC OSCILLATOR

The harmonic oscillator uses a timing reference, a passive circuit whose transfer function H has at least two poles, to provide the constants that determine the oscillator frequency. Figure 12.2 shows the oscillator's mathematical model.

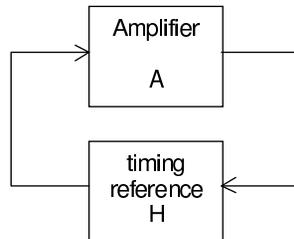


Figure 1.2 Figure 12.2: Simple model of the harmonic oscillator

The timing reference defines the frequency where the oscillation conditions can be met. The amplifier circuit provides the gain required for start-up and steady state oscillation:

$$\begin{aligned} |AH| &> 1 \text{ and } \arg(AH) = 0 \text{ for start-up} \\ |AH| &= 1 \text{ and } \arg(AH) = 0 \text{ in the steady state} \end{aligned}$$

Various passive circuits can be used as timing reference in harmonic oscillators [3]. These circuits have poles that can be either real or complex. In this chapter we address oscillators whose timing reference is characterized by two complex conjugated poles and one real zero. This pole-zero pattern is usually encountered in the frequency selective resonators and resonator circuits used as timing reference in low-noise oscillator circuits.

A mechanism is required to reduce the loop gain as the oscillation amplitude increases in order to guarantee a well-defined steady state for the oscillator. Two possibilities are available:

- amplitude regulator (ALC)
- well defined non-linearity in active part

Figure 12.3 illustrates the two approaches.

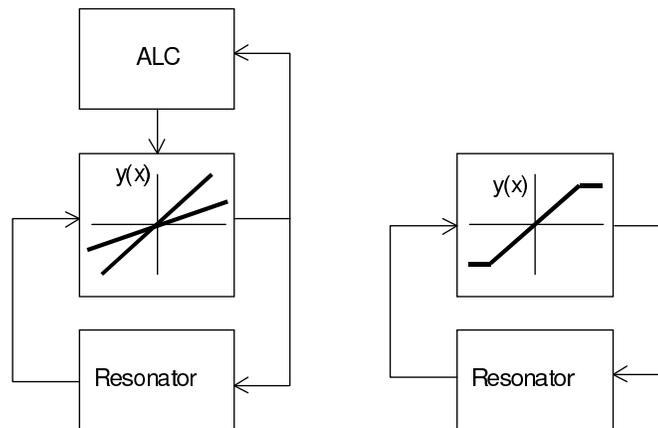


Figure 1.3 Figure 12.3: Oscillator amplitude control using an ALC loop or a well-defined non-linearity in the amplifier part.

The first solution measures the amplitude of the oscillator output signal and uses a feedback structure to control the amplifier gain. The amplifier always operates in its linear region. Oscillators with ALC circuits yield

- accurate amplitude

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- low harmonic distortion

Amplitude regulators or Automatic Level Control (ALC) circuits were used in the very first quartz oscillators for watch applications [4] and have regained popularity recently [5]. Oscillator phase noise originating from the down-conversion of noise at harmonics of the oscillator frequency does not occur in this type of oscillator. The challenge in designing these circuits is to minimize the noise added by the ALC circuit.

The alternative way to go is to implement a well-defined non-linearity in the amplifier part of the oscillator to control the oscillation amplitude. This approach results in simpler circuits whose phase noise performance is slightly degraded with respect to the linear oscillator. Figure 12.4 shows two circuits that can be used to implement a controlled non-linearity [3].

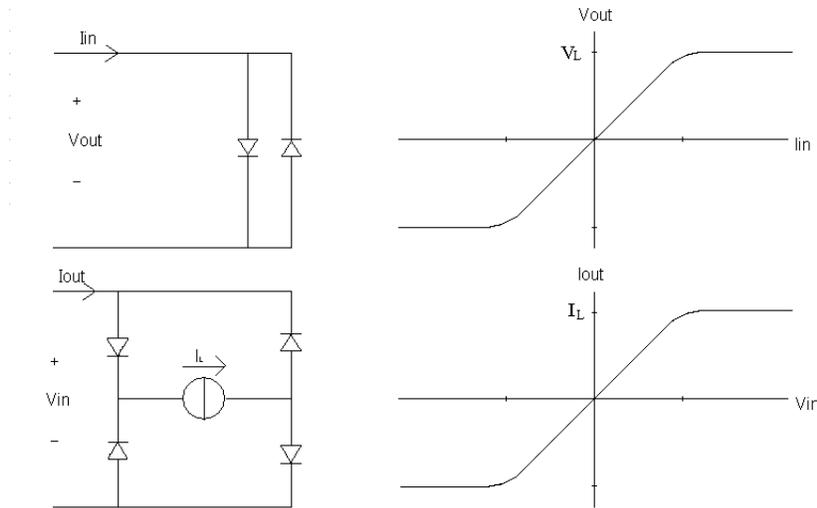


Figure 1.4 Figure 12.4: Two examples of a controlled non-linearity [3]

1.3 SECOND ORDER RESONATOR CONFIGURATIONS

A resonator is a linear frequency selective system that stores energy in one or several resonance modes. The resonance is characterized by its frequency f_0 and quality factor Q defined as the ratio between stored and dissipated energy per oscillation period T_0 .

$$Q = 2\pi \frac{E_{stored}}{E_{dissipated}} = \frac{E_{stored}}{P_{res} T_0} \quad (1.2)$$

The most commonly used resonators in harmonic oscillators have a band-pass transfer function H described by two complex poles and one real zero. With $p = j\omega$, it follows

$$H = H_0 \frac{\frac{\omega_0}{Q}p}{p^2 + \frac{\omega_0}{Q}p + \omega_0^2} = \frac{H_0}{1 + jQ\frac{\omega}{\omega_0} - jQ\frac{\omega_0}{\omega}} \quad (1.3)$$

Some properties of an oscillator signal, like its phase noise, are usually presented as a function of the frequency offset $\Delta\omega$ from the oscillator frequency ω_0 . A performance comparison between resonators or oscillators operating at different frequencies also requires normalization with respect to the oscillator frequency. These two features can be easily obtained when the frequency ω is replaced by a variable named detuning ν defined as

$$\nu = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \approx 2\frac{\omega - \omega_0}{\omega_0} = 2\frac{\Delta\omega}{\omega_0} \quad (1.4)$$

The resonator impedance can now be rewritten as

$$H = \frac{H_0}{1 + jQ\nu} \quad (1.5)$$

This is a convenient form for further mathematical manipulations. The 2nd order resonator is fully characterized by its resonant frequency f_0 , quality factor Q and the maximum value of its transfer function H_0 . Figure 12.5 shows the magnitude and phase of the 2nd order resonator transfer function. This transfer function can describe either a one-port or a two-port.

Figure 12.6 shows such a resonator circuit made out of a series connection of an inductor L , a capacitor C , and an equivalent series loss resistance R_s . In practical resonators, inductor losses usually dominate and R_s is associated with the inductor.

When this resonator is driven by a voltage source V , the resonator admittance Y equals

$$Y = \frac{I}{V} = \frac{1}{R_s \left(1 + j\omega\frac{L}{R_s} - j\frac{1}{\omega R_s C}\right)} = \frac{1}{R_s} \frac{1}{1 + jQ\frac{\omega}{\omega_0} - jQ\frac{\omega_0}{\omega}} = \frac{1}{R_s} \frac{1}{1 + jQ\nu} \quad (1.6)$$

It can be seen that the inductor and capacitor voltage are a factor Q larger than the driving voltage. The resonant frequency f_0 , resonator quality factor Q and resonator power P_{res} are given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (1.7)$$

$$Q = 2\pi \frac{E_{\text{stored}}}{E_{\text{dissipated}}} = 2\pi \frac{1/2 L \hat{I}^2}{1/2 \hat{I}^2 R_s} f_0 = \frac{\omega_0 L}{R_s} = \frac{1}{R_s} \sqrt{\frac{L}{C}} \quad (1.8)$$

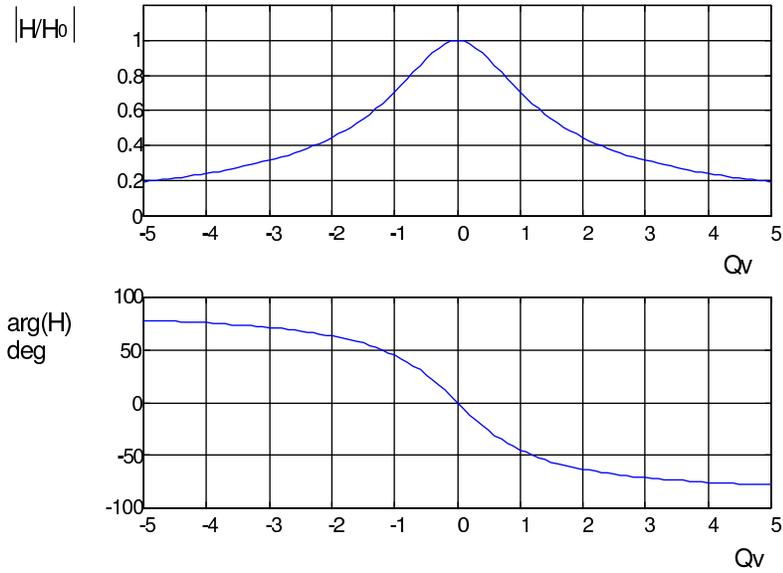


Figure 1.5 Figure 12.5: Transfer function of a second order resonator

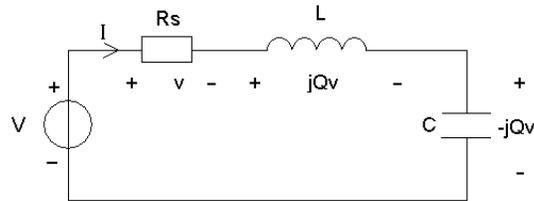


Figure 1.6 Figure 12.6: A series resonant LC circuit

$$P_{res} = \frac{1/2 V^2}{R_s} = 1/2 \hat{I}^2 R_s \quad (1.9)$$

When the same passive components are connected in parallel and driven by a current source as shown in Figure 12.7, the impedance Z has a resonant character.

For frequencies $\omega \approx \omega_0$, the series connection of inductance L and series loss resistance R_s can be replaced by an inductance L_p in parallel with an equivalent parallel loss resistance R_p as shown in Figure 12.8.

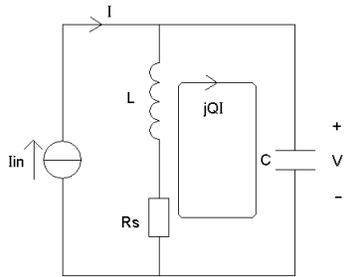


Figure 1.7 Figure 12.7: A parallel resonant LC circuit

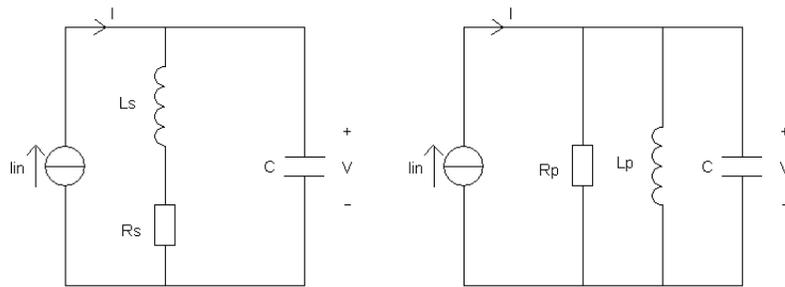


Figure 1.8 Figure 12.8: Equivalent circuits (near ω_0)

For the parallel resonant circuit, the internal current flowing through L_p and C is a factor Q larger than the external current. The values for the inductance L_p and loss resistance R_p are

$$R_p = (1 + Q^2) R_s \approx Q^2 R_s \quad (1.10)$$

$$L_p = \frac{(1 + Q^2)}{Q^2} L_s \approx L_s \quad (1.11)$$

This yields for the impedance of the parallel resonant circuit

$$Z = \frac{V}{I} = \frac{R_p}{1 + j\omega R_p C - j\frac{R_p}{\omega L}} = \frac{R_p}{1 + jQ\frac{\omega}{\omega_0} - jQ\frac{\omega_0}{\omega}} = \frac{R_p}{1 + jQv} \quad (1.12)$$

The resonant frequency, quality factor and resonator power are given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (1.13)$$

$$Q_p = 2\pi \frac{E_{stored}}{E_{dissipated}} = 2\pi \frac{1/2 L (Q\hat{I})^2}{1/2 (Q\hat{I})^2 R_s} f_0 = \frac{\omega_0 L}{R_s} = \frac{R_p}{\omega_0 L} = R_p \sqrt{\frac{C}{L}} \quad (1.14)$$

$$P_{res} = \frac{1/2 V^2}{Q^2 R_s} = 1/2 \hat{I}^2 Q^2 R_s \quad (1.15)$$

It is a fact that for meeting an oscillator phase noise specification, a minimum resonator power is required. Figure 12.9 shows two basic oscillator circuits using either a series or parallel resonator circuit. Which circuit is to be preferred given this minimum resonator power?

When a parallel resonant circuit is used, this results in a higher voltage swing across the resonator. This may be the preferred solution when the active circuit has enough voltage headroom.

When a series resonant circuit is used, this results in higher current required for driving the resonator. This may appear the only choice when supply voltage is low and large voltage headroom is not available.

1.3.1 Resonator tapping

In a resonator practical oscillator circuit, where the resonator components are imposed by e.g., IC technology, neither of the two extremes shown in Figure 12.9 may yield a

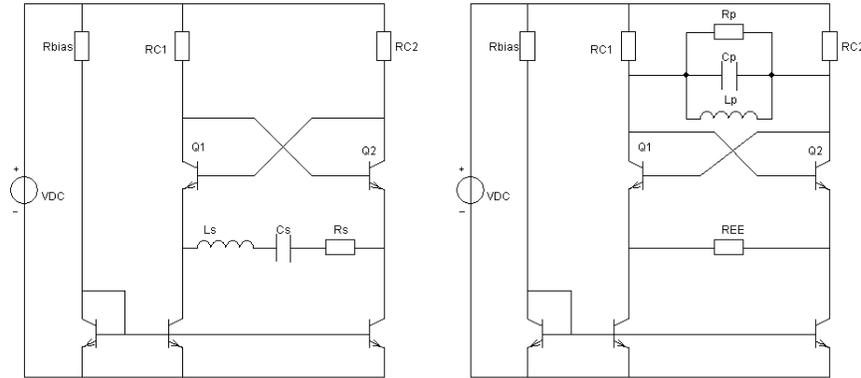


Figure 1.9 Figure 12.9: Two basic oscillator circuits using one-port resonators: a) series resonant and b) parallel resonant

circuit with the required specifications. Resonator tapping [3] transforms the resonator impedance into an intermediate value R_T with the restriction

$$R_s < R_T < R_p = Q^2 R_s \tag{1.16}$$

Tapping can be interpreted as a sliding transition between the series and parallel resonant circuit. Figure 12.10 shows how to implement capacitive resonator tapping for both series and parallel resonant circuits.

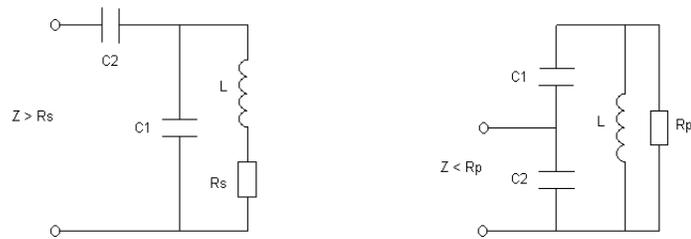


Figure 1.10 Figure 12.10: Capacitive resonator tapping examples for series and parallel resonant circuits.

Tapping does not have to be capacitive. Inductive tapping can be implemented by

- two separate uncoupled inductors

- one single inductor with a real physical tap.

The choice between inductive and capacitive tapping is in principle free. In practice, the choice depends on the availability of components, their quality factor (which may be a function of the component value), and the available board space or chip area.

Very often, the advantage is going in the direction of capacitive tapping, or inductive tapping using a physical tap. The latter solution adds no extra components, however, it requires that the tap is accessible.

Tapping of a one-port resonator still yields a one-port resonator. The additional node created by tapping can be used to change the resonator into a two-port. This can be advantageous in some situations as will be shown in the section dealing with practical oscillator design.

1.3.2 Two-port resonators

A more flexible approach is to use a two-port resonator structure where separate input and output terminals exist. The use of a two-port resonator structure makes resonator input and output impedance independent of each other. The first can be chosen for maximum resonator power whereas the latter can be optimized for minimum noise [3].

Figure 12.11 shows an example of a two-port resonator that can be interpreted as a parallel resonant circuit tapped on both the input and output port. This resonator combined with a transconductance amplifier stage is usually referred to as a Collpitts oscillator.

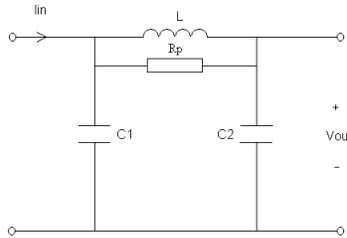


Figure 1.11 Figure 12.11: Two-port resonator example

Its transfer function at resonance H_0 , its resonant frequency f_0 and its quality factor Q are given by

$$H_0 = -R_p \frac{C_1}{C_1 + C_2} \frac{C_2}{C_1 + C_2} \quad (1.17)$$

$$Q_p = \frac{R_p}{\omega_0 L} \quad (1.18)$$

$$f_0 = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}} \tag{1.19}$$

When the inductor is replaced by a quartz crystal, and an inverter circuit is added, a widely used (not necessarily the best) clock oscillator emerges. Figure 12.12 shows the resulting circuit. The oscillator frequency is in between the quartz’s resonance and anti-resonance frequency, where its impedance is inductive.

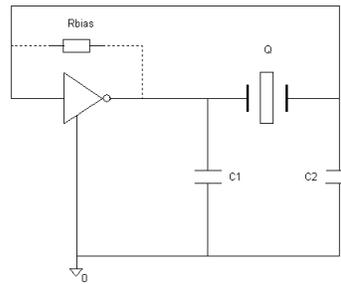


Figure 1.12 Figure 12.12: A legendary clock oscillator circuit, the quartz operates in its inductive region

1.4 PRACTICAL DESIGN EXAMPLES

This section presents two oscillator designs for different applications realized in different IC technologies. The common factor is the operating frequency of 900 MHz. Table 12.1 shows the most important characteristics of the two oscillator circuits.

Table 1.1 Table 12.1: Main requirements for the two oscillator circuits

Oscillator characteristic	Oscillator 1	Oscillator 2
IC Technology	Bipolar	CMOS
Resonator	Off-chip, Q = 25, one-port	On-chip, Q ≈ 5, two-port
Phase noise	-100 dBc/Hz @ Δf = 100 kHz	-101 dBc/Hz @ Δf = 25 kHz
Supply current	< 1 mA	< 10 mA
Supply voltage	1.5 V	3 V

First we will calculate the required resonator power for the two applications. Manipulation of Leeson’s formula [6], and taking into account the frequency folding as a result of the small-signal loop gain $AH_o > 1$, yields for the resonator power P_{res}

$$P_{res} = 2kT \frac{10^{-\frac{L(\nu)}{10}}}{\nu^2} \frac{NF \cdot AH_0}{Q^2} \tag{1.20}$$

In this formula $L(\nu)$ is expressed in dBc/Hz. The minimum required resonator power occurs for a hypothetical linear oscillator with a noise-free active part. In that case the thermal noise energy kT of the resonator determines the phase noise.

Figure 12.13 shows the results for the two practical oscillators. Since oscillator 2 has a more severe phase noise requirement and its resonator Q is lower, it requires a resonator power that is 400 times higher (16 due to $L(\nu)$ and 25 due to Q). 1.2 mW versus 3 μ W.

In a real world oscillator, this minimum value is not sufficient. Especially when the oscillator circuits used are not linear oscillators with an ALC circuit but circuits with a controlled non-linearity to fix resonator power. The small-signal loop gain AH_0 of the oscillator is chosen equal to two resulting in reliable start-up and rejection of AM noise [2]. Moreover, the noise factor of the active circuit cannot be neglected and may be as high as 5 (7 dB). This results in a resonator power that may be 10 times higher than the theoretical minimum value.

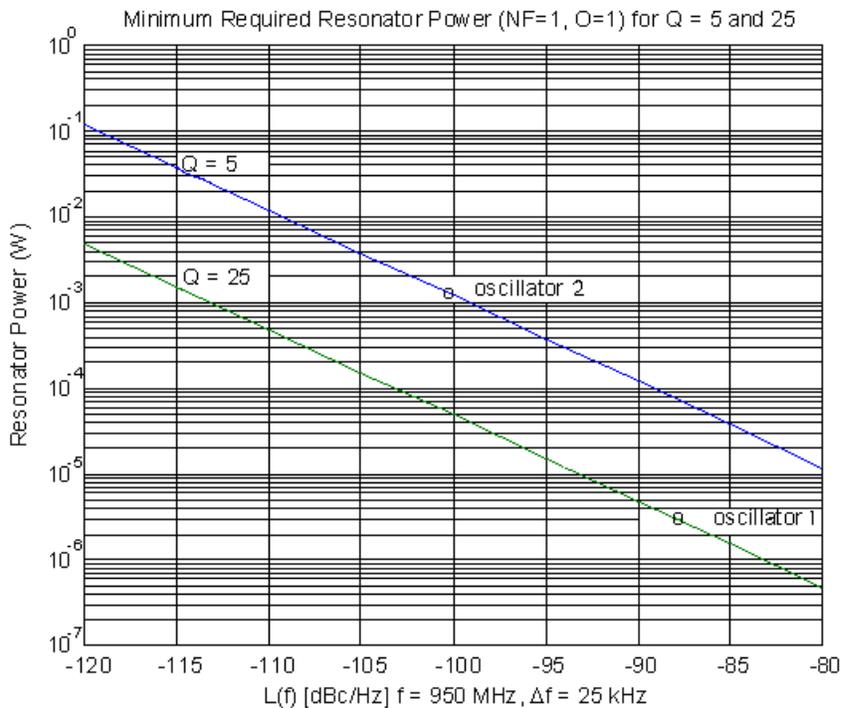


Figure 1.13 Figure 12.13: Minimum required resonator power.

1.4.1 Oscillator in bipolar technology using off-chip resonator

The major challenge in this oscillator design is constituted by the external tank circuit. It has a high resonator quality factor but the fact that it is off-chip complicates the resonator structure. Figure 12.14 shows the equivalent circuit seen by the on-chip active circuit. It comprises the on-chip bond pads, ESD diodes, bond wires, the package and finally the external resonator. The bond wires constitute high-quality inductors ($Q \approx 100$). Together with the on-chip capacitance C_{int} , a second parallel resonance occurs that may be stronger than the desired one defined by the external tank circuit.

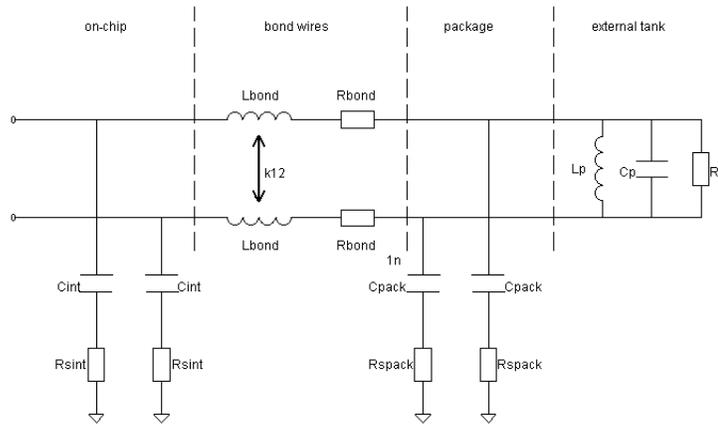


Figure 1.14 Figure 12.14: Complete resonator structure seen by the on-chip oscillator circuit.

Figure 12.15 shows the magnitude and phase of the impedance seen on-chip by the active circuit. The undesired mode at about 4 GHz is stronger than the wanted mode when the series resistance of the on-chip capacitance C_{int} is sufficiently low.

This will result in an unwanted oscillation frequency of 4 GHz. Lowering the bandwidth of the active circuit by adding a low-pass filter as shown in Figure 12.16, solves this problem.

Resistors R_{B1} , R_{B2} and capacitor C_1 lower the loop gain at 4 GHz thus ensuring the correct oscillation frequency of this oscillator circuit. The external tank circuit is constituted by SMD components of the following values:

$$\begin{aligned}
 L_p &= 5 \text{ nH (} j33 \Omega \text{ at 1 GHz)} \\
 C_p &= 5 \text{ pF} \\
 R_p &= 800 \Omega
 \end{aligned}$$

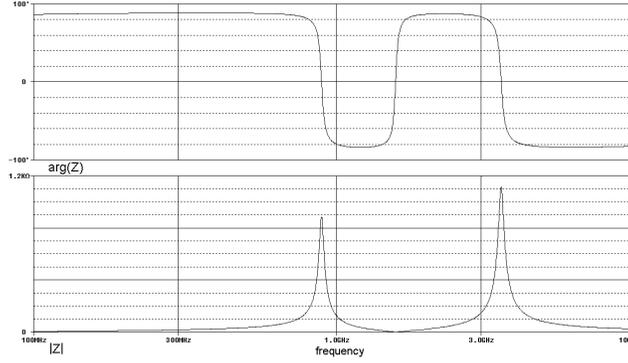


Figure 1.15 Figure 12.15: Resonator impedance seen on-chip.

The peak resonator current is $300 \mu\text{A}$ resulting in a resonator power $P_{\text{res}} = 40 \mu\text{W}$. Voltage swing equals 240 mV peak. This swing is compatible with the differential pair. No resonator tapping is required.

The negative impedance Z_N seen by the external tank circuit equals

$$Z_N = -R_N = - \left(R_{EE} + 2 \frac{kT}{q} I_E \right) \quad (1.21)$$

Substituting $300 \mu\text{A}$ for the emitter current I_E of each transistor yields an impedance of -370Ω . This corresponds to an overdrive $AH_0 = 2.2$.

Phase noise can be calculated using the modified Leeson's formula taking into account the increase of phase noise due to the non-linearity of the active element. Calculation yields -101 dBc/Hz at 100 kHz distance from the carrier.

$$L(\nu) = 10^{10} \log \left[\frac{2kT}{P_{\text{res}}} \frac{NF}{Q^2 \nu^2} AH_0 \right] \text{ dBc/Hz} \quad (1.22)$$

The oscillator was realized in a bipolar technology with a transition frequency $f_T = 20 \text{ GHz}$. Measurements with various external tank circuits showed no parasitic oscillations in the GHz range. Oscillator phase noise at 100 kHz distance from the carrier was found to be -102 dBc/Hz at an oscillator frequency of 767 MHz and -95 dBc/Hz at an oscillator frequency of 1044 MHz.

1.4.2 Oscillator in CMOS technology using on-chip resonator

The second oscillator is realized in a CMOS technology and uses on-chip Inductors and varactor diodes. This puts some limitations on the available component values. As an example, Figure 12.17 shows the available on-chip inductor values and their respective quality factor. It can be seen that the quality factor is more or less proportional to the square root of the inductance value.

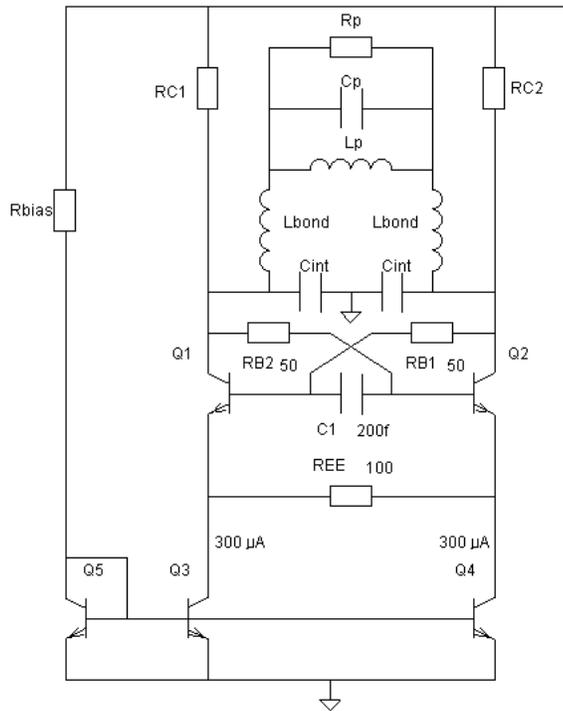


Figure 1.16 Figure 12.16: Schematic diagram of the bipolar oscillator; components L_p , C_p and R_p constitute the external tank circuit.

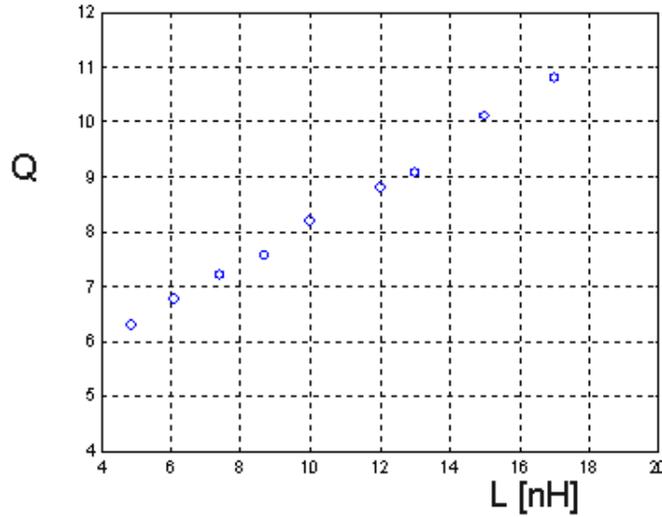


Figure 1.17 Figure 12.17: Available on-chip inductors for oscillator 2

A resonator power of 10 mW is required for this oscillator. Figure 12.18 shows the resulting resonator voltages and currents for one-port series and parallel resonant circuits.

It can be seen that the series resonant circuit requires considerable current whereas the parallel resonant circuit requires a voltage swing at the limit of available voltage headroom- even for the lowest inductor value. Considering the wish for low current consumption a tapped parallel resonant circuit with low inductance value was chosen to reduce the swing at the output of the active circuit.

Figure 12.19 shows the tapping scheme that was used. Not only is the resonator tapped, but it is also used as a two-port since the input of the amplifier is connected to the top of the resonator.

The transfer function for the two-port resonator is the same as that of the one-port.

$$H = \frac{V_{out}}{I_{in}} = \frac{R_p}{1 + jQv} \quad (1.23)$$

As a result the small-signal loop gain AH_o of the oscillator is not lowered by the tapping action, which is advantageous for both current consumption and oscillator noise. However, the input impedance seen at the input of the two-port equals $1/2R_p$. This results in half the voltage swing.

Figure 12.20 shows the respective transfer functions of the two resonator circuits. Figure 12.21 shows the complete oscillator schematic diagram. A differential resonator structure helps to further increase voltage headroom. Capacitors C_{DD1} , and C_{DD2} together with resistor R_{DD2} constitute the on-chip supply decoupling. A 45 pF capacitor

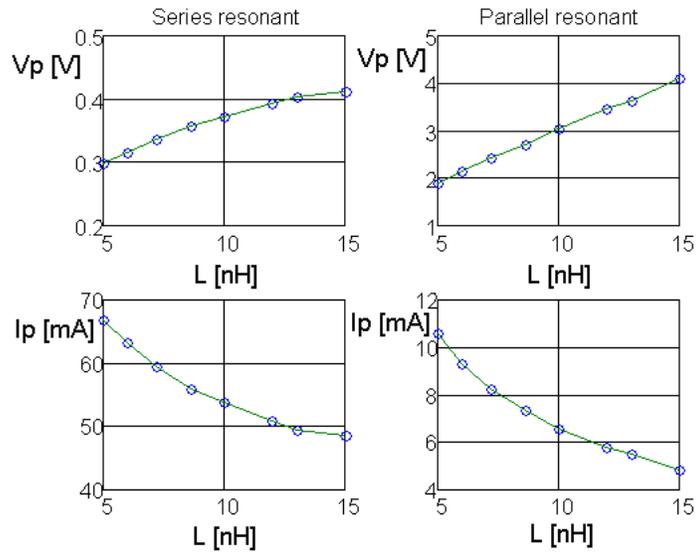


Figure 1.18 Figure 12.18: Resonator voltage and current for series and parallel resonant circuits

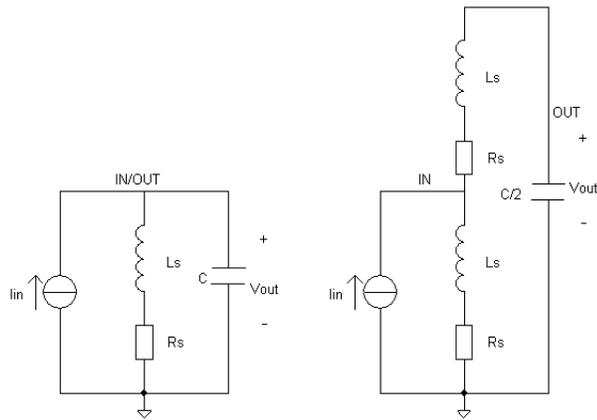


Figure 1.19 Figure 12.19: A one-port and a two-port circuit with the same transfer function yet different input voltage swing.

has an impedance of $-j4 \Omega$ at 900 MHz. The series resistance R_{DD2} lowers the quality factor of the decoupling capacitance and helps to suppress resonance phenomena caused by the inductance of the power supply bond wire.

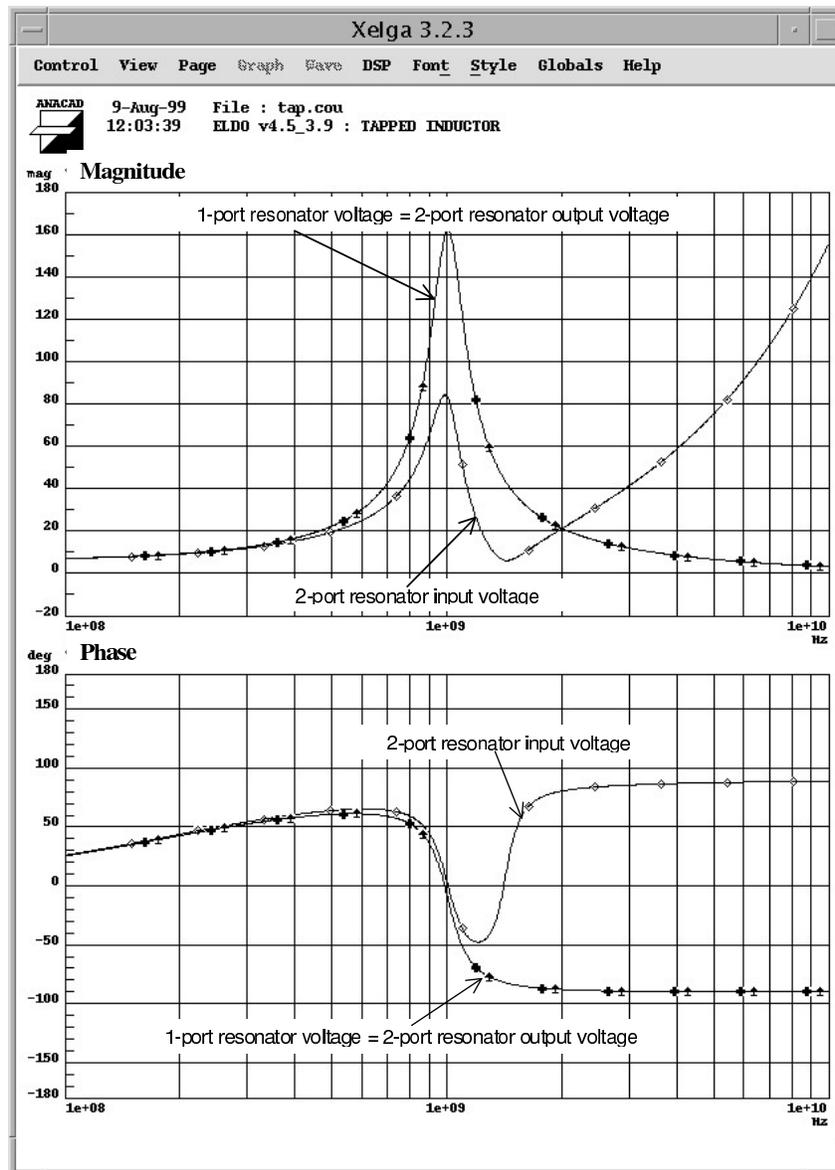


Figure 1.20 Figure 12.20: Transfer function of one-port and two-port resonator with reduced input voltage swing.

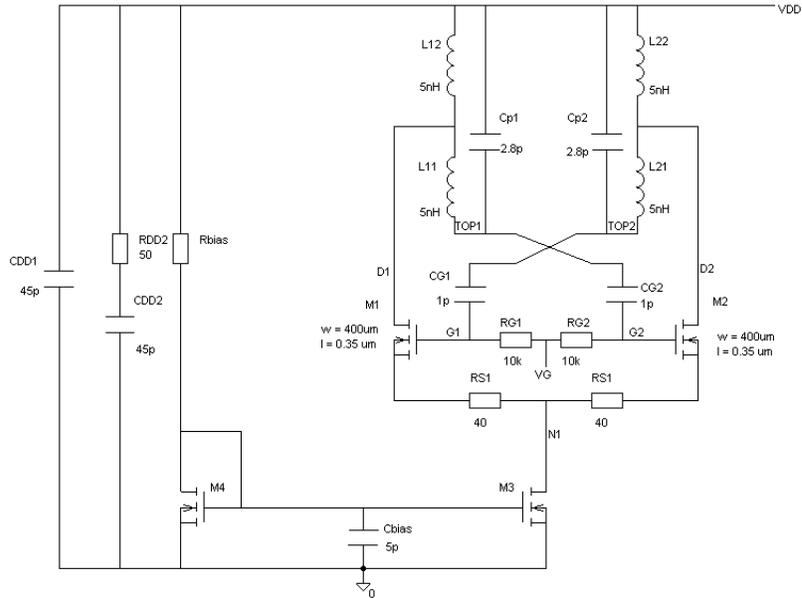


Figure 1.21 Figure 12.21: Complete oscillator schematic.

Figure 12.22 shows some of the waveforms occurring in this oscillator circuit.

One may wonder whether the resistive source degeneration by resistors R_{S1} and R_{S2} does not degrade the noise performance of the circuit. Figure 12.23 shows the simulated noise of a differential pair for various transistor sizes. The equivalent noise resistance is the hypothetical resistor value that results in the same current noise.

It can be seen that the output white noise increases with the transistor width, since the transconductance g_m is proportional to the transistor width. The $1/f$ noise at the input decreases with increasing transistor width. Figure 12.24 shows the effect of resistive degeneration upon the noise.

Comparison of the white output noise level of the differential pair with transistor width $W = 50 \mu\text{m}$ and that of the resistively degenerated pair with $W = 400 \mu\text{m}$, shows exactly the same output noise value, equivalent to a 120Ω resistor. Comparison of the $1/f$ input referred noise however, yields a gain of 8 dB. Therefore, we expect better close-in phase noise performance from the oscillator with the larger transistors and resistive degeneration.

The oscillator noise figure can be deduced from the white part of the output noise

$$NF = \frac{R_p}{R_{noise}} = 3. \tag{1.24}$$

The oscillator was integrated in a $0.35 \mu\text{m}$ CMOS process. Figure 12.25 shows the measured phase noise. It can be seen that total phase noise equals -93 dBc/Hz at 25

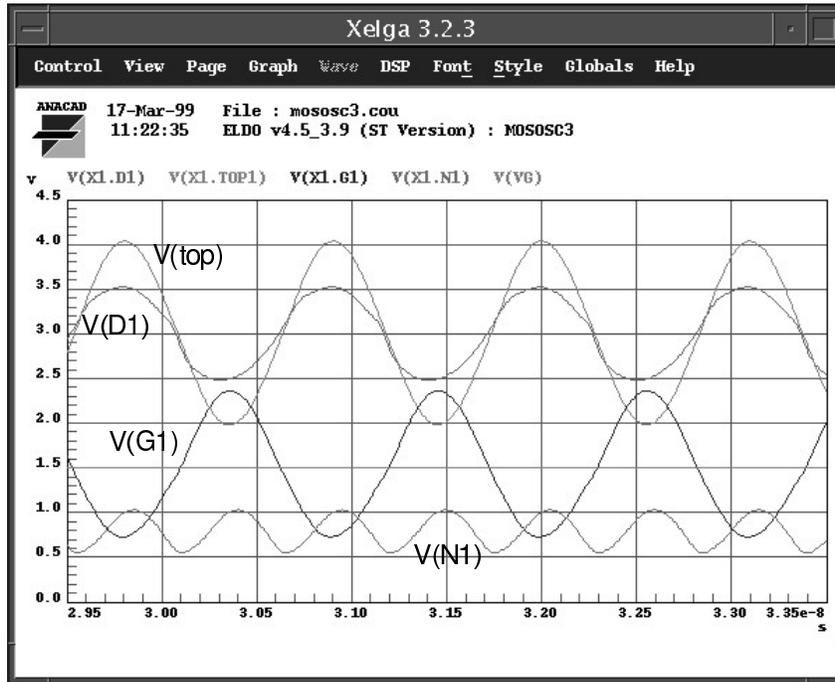


Figure 1.22 Fig. 12.22: Waveforms in the oscillator circuit; node N1 is at the connection of the two source degeneration resistors.

kHz offset from the carrier. The contribution of the white noise equals -100 dBc/Hz which is close to the calculated value of -101 dBc/Hz.

1.5 CONCLUSIONS

Two oscillator circuit examples clearly illustrate that it is possible to design oscillator circuits using either external or on-chip inductors. The low quality factor of on-chip inductors results in high resonator power and overall power consumption. A good alternative is to use an inductor on a separate substrate flipped onto the chip or an inductor etched on the PCB of the package (BGA).

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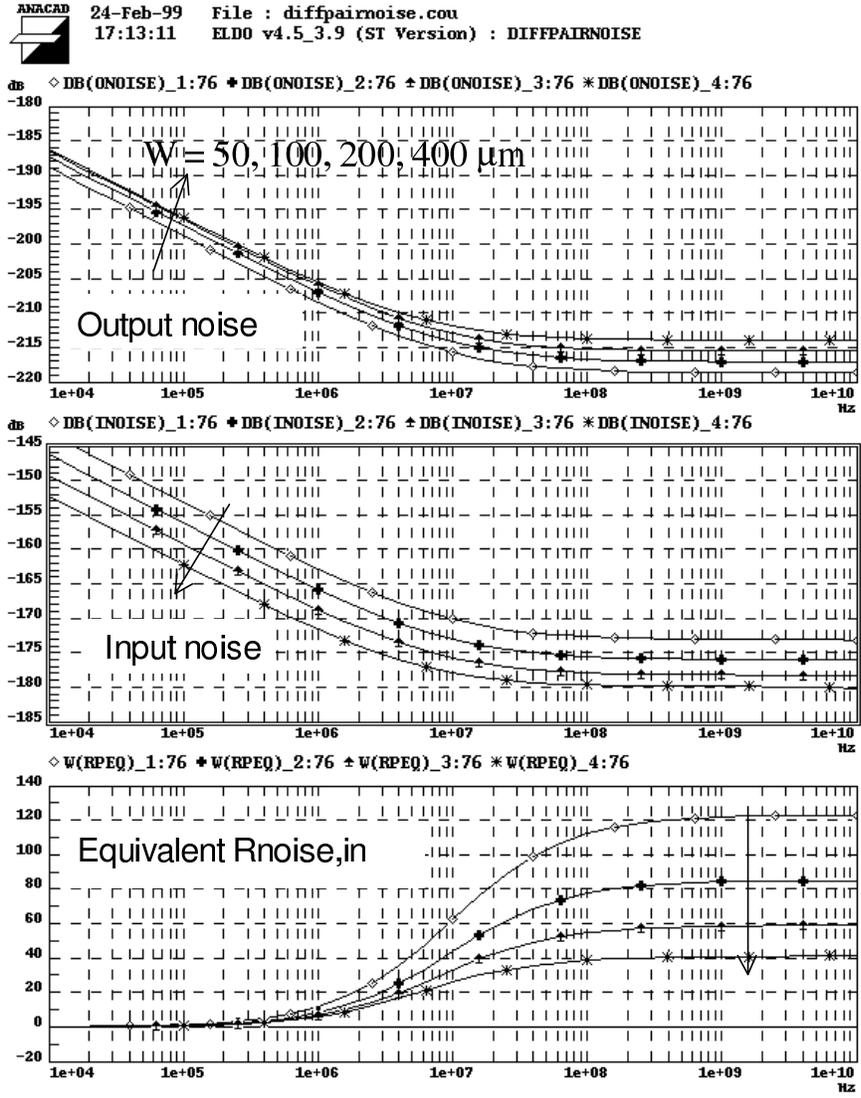


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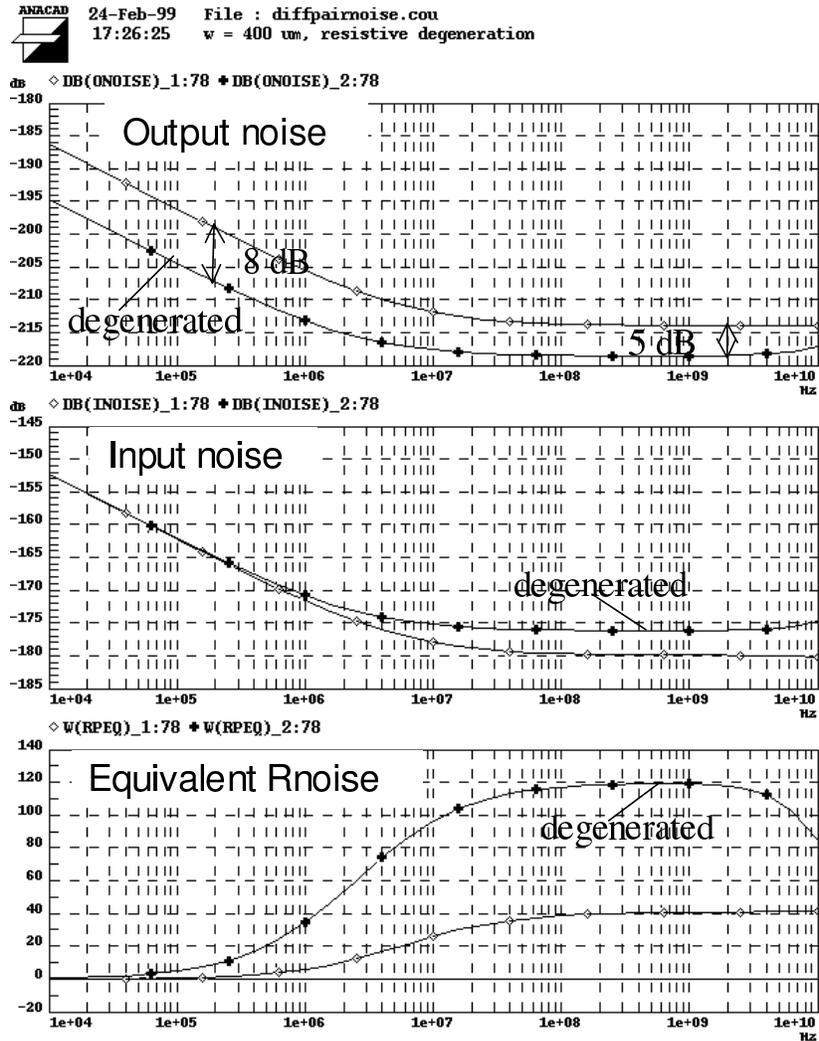


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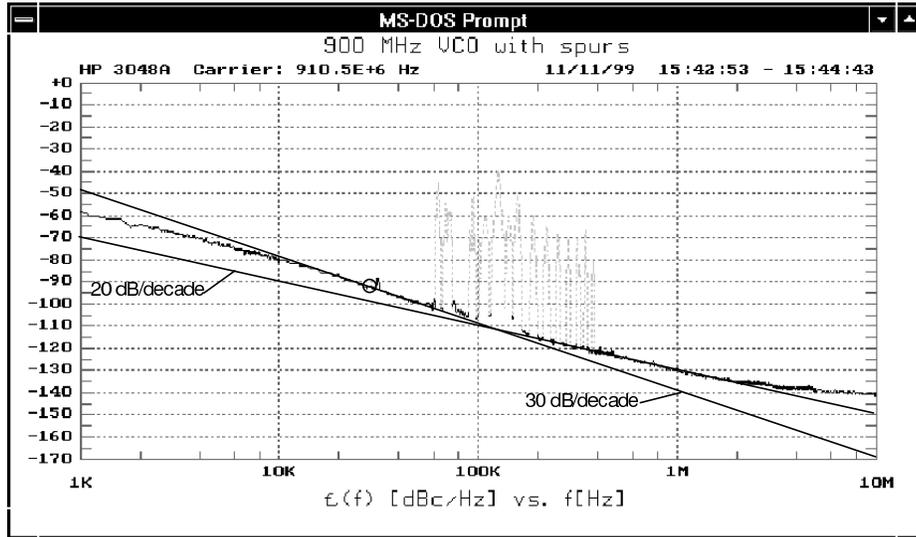


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