A 2.7 V DECT RF-Transceiver/Synthesizer/Modem Chip Set

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Abstract

The BiCMOS DECT chip set described here, consists of a RF transceiver IC containing LNA, Mixer, Small Power Amp and offset PLL, a synthesizer IC, featuring zero blind-slot operation, and a modem IC containing a fully integrated modulator and demodulator. The set performs all RF/IF signal processing between Base-Band Controller and RF Power Amplifier/Antenna Switch.

Introduction

The Digital Enhanced Cordless Telecommunications (DECT) standard has been around for some time now and recently chip sets and radio frequency (RF) transceiver integrated circuits (IC) for the design of the radio part (RP) of hand sets and base stations have become available. A closer look at these chips [1][2] shows that the number of external components and tuning processes needed is rather high. RF voltage controlled oscillators (VCO) are often partially or totally off chip, use ceramic resonators and run at half the transmit frequency, leading to the use of frequency doublers and "fundamental suppressing" filters in the transmit path. Moreover, "open-loop" modulation is often performed by supplying an analog Gaussian filtered data signal to the RF VCO. The frequency deviation and frequency pulling caused by power-amplifier switching is not easily controlled. Transmitter chains using up-conversion architectures [3] have to be connected to SAW filters, in order to get rid of unwanted harmonics and image frequencies. The available synthesizers are mostly dual frequency synthesizers with external loop filters. They exhibit large lock-in times, due to low reference frequencies and open-loop modulation and have to be switched on long before a transmit or receive burst occurs (blind slot operation). The available integrated receive chains, mostly with off-chip low noise amplifiers (LNA), are straight forward super-hets with quadrature demodulators that require bulky external tank-circuits. The 2.7 V DECT chip set presented here addresses most of the problems described above, has been realized in a 12GHz 0.8u BiCMOS process and consists of a Transceiver IC, Modem IC and a Synthesizer IC. To build a DECT radio part requires this chip set, ceramic/SAW filters, a power amplifier, antenna switch and a small amount of external passives.

Architecture

Fig. 1 shows the developed chip set in an application diagram for a typical DECT RP. The receive chain is a super heterodyne with two intermediate frequencies (IF) at 112.320 MHz and

1.728 MHz. The second low IF offers the advantage of easy implementation of filtering and amplifying stages and of implementing a completely digital demodulator. No external passive components are needed. The transmit chain consists of digital look-up table-based quadrature base-band Gaussian Minimum Shift Keyed (GMSK) signal generators followed by a quadrature modulator, translating base-band to 110.592 MHz. This frequency is very close to the receive-chain IF, so no dual frequency synthesizer and wide band VCOs are needed. A second advantage is that the frequency deviation is precisely controlled. The IF signal is fed to an offset Phase Locked Loop (PLL) followed by the small power amplifier (SPA). The SPA drives the external power amplifier. The offset PLL offers a number of advantages; Firstly, RF filtering is reduced, since no RF image frequency is present and the harmonic distortion of the RF VCO is low. Secondly, a large loop bandwidth, needed to track the GMSK modulated reference frequency, filters out-of-band signals and reduces VCO frequency pulling caused by switching power amplifiers.

The transceiver IC contains a LNA and Mixer for receive and the offset PLL for transmit functions. Package parasitics cause significant effects on the circuit performance at the DECT RF frequencies (1.7-1.9 GHz). Extensive measurements and field simulations were performed to obtain an accurate package model. Taking into account the dummy paddle leads at the corner areas resulted in a very good agreement between measured and simulated package characteristics [4]. The field simulations included the actual bonding conditions and the presence of the PCB and solder dots (Fig.2). The LNA is optimized for constant gain under varying process parameters while the on-chip inductance seen on the chip photograph has been used to degenerate RF-gain at very high frequencies to avoid LNA instability caused by package parasitics. The 110.592 MHz GMSK-modulated signal used as the offset PLL's reference signal is rather high and offered a challenge for the design of the Phase Frequency Detector's (PFD) charge pump. Fig. 5. Shows the bipolar charge pump. The bipolar switches are driven by Common Mode Logic (CML) gates. The dynamic level shifters T1,T1a,R1, R1a and T2, T2a, R2, R2a are controlled by the VCO control voltage. Together with low voltage current sources, the output range is increased to [VDD-0.3, VSS+0.7]. This leaves about a minimum 1.7 V range, enough for the 50 MHz/V sensitive VCO. The VCO is a cross-coupled quad-bipolar oscillator with amplitude-control circuits and on-chip reverse-biased bipolar varactors and is connected to a simple printed circuit board (PCB) strip-line resonator. The pads, optimized to reduce parasitic substrate resistance, the package leads, the bondwires and the stripline resonator on the PCB were included in the design process. The model is partly shown in fig. 3. Phase noise performance has been optimized (Fig. 4) and the size of the varactors were defined to reach the desired tuning gain. It has been found that amplitude control, included to generate a defined output amplitude level, increases the power level in the resonator with decreasing resonator quality factor and reduces phase-noise performance sensitivity to the resonator quality factor. To prevent the offset PLL from latching on the image frequency, the RF VCO is pre-charged to its highest frequency during start-up.

The **synthesizer IC** is, apart from the RF VCO's strip line, completely integrated and programmable via a 3-wire bus. The main design goal was to be able to use it in zero blind-slot operation, requiring it to lock to within 50kHz of the carrier in less than 25us. To achieve this, a calibration is performed at start-up that stores the loop filter voltages of each individual channel to be used for pre-charging the loop filter upon channel switching. Fig. 6 shows the

measured response of the synthesizer, while switching from channel 5 to channel 6 ($\Delta f = 1.728$ MHz). After achieving lock, the loop filter voltage is re-calibrated for future use, thus compensating for temperature and voltage supply drift. Several options can be programmed through the 3-wire interface such as: 1. Selection of the minimum loop bandwidth upon lock, thus easing the trade-off between switching speed and spurious output. 2. Phase alignment of the reference and feedback divider outputs after power-down, for fast lock after power-down (<50us) [3]. 3. The VCO can be switched off, for use of an external VCO. 4. Eight possible charge pump currents and loop filter damping resistors can be selected (useful together with option 3.).

In the **modem IC**'s receive chain, the mixer translates the received signal to 1.728 MHz, which is equal to one DECT channel spacing. This signal is fed into the amplifier/filter/limiter. Band limiting and gain is realized by four continuous time AC-coupled Sallen-and-Key filter amplifier stages, resulting in symmetrical group delay, eighth-order roll off and a gain of more than 100 dB. A 80 dB dynamic range RSSI is included and analog RSSI output is available. The quadrature discriminator with digital delay line is followed by a low pass circuit and a digital slicer with frequency-deviation measurement feature. A temperature-compensated peak-hold RSSI value and the frequency deviation value are in digital form available through the 3-wire bus. The transmit chain consists of digital look-up table-based quadrature base-band GMSK signal generators followed by a quadrature modulator, translating base-band to 110.592 MHz. One PLL generates all frequencies necessary for transmit and receive modes. The VCO includes an amplitude control circuit and runs at twice the transmit frequency. This avoids oscillator pick-up and eases the generation of quadrature signals. Fig. 7 shows the VCO with amplitude control and table 1 summarizes measured performance of the chip set and fig. 8 through 9 show the chip photographs.

Acknowledgments

References

[1] Heinen, S., et al., "A 2.7V 2.5GHz Bipolar Chipset for Digital Wireless Communication," ISSCC Digest of Technical Papers, pp. 306-307, Feb., 1997.
[2] LMX 3161 data sheet, National Semiconductor, September 1996.
[3] Sato, H., et al., "A 1.9GHz Single Chip IF Transceiver for Digital Cordless Phones, " ISSCC Digest of Technical Papers, pp. 342-343, Feb., 1996.
[4] F. Mernyei, "Measurement and Field Simulation Based Characterization of Plastic IC Packages," Proc. of the IEEE 6th Topical Meeting on Electrical Performance of Electronic Packaging, pp181-184, Oct., 1997

General:	
Supply voltage	2.7 to 4.5V
System ref. frequency	13.824 MHz
RF channel switching time	<25µs for ±50 kHz
Radio interface	digital
Standby current:	<150 µA (on chip X-TAL OSC)
RX- chain	
Noise figure	< 6 dB
RSSI measurement range	80 dB
Freq. Deviation measurement range	±150 kHz
RX current consumption	113 mA at 3.6 V
RX turn-on time	≈60 µs
TX- chain	
Differential RF output power	+3 dBm
Modulation format	GMSK
TX Spurious	<-71 dBc @ ±3rd channel
TX current consumption	163 mA at 3.6 V
TX- turn-on time	≈60 µs

Table 1. DECT chip-set performance summary
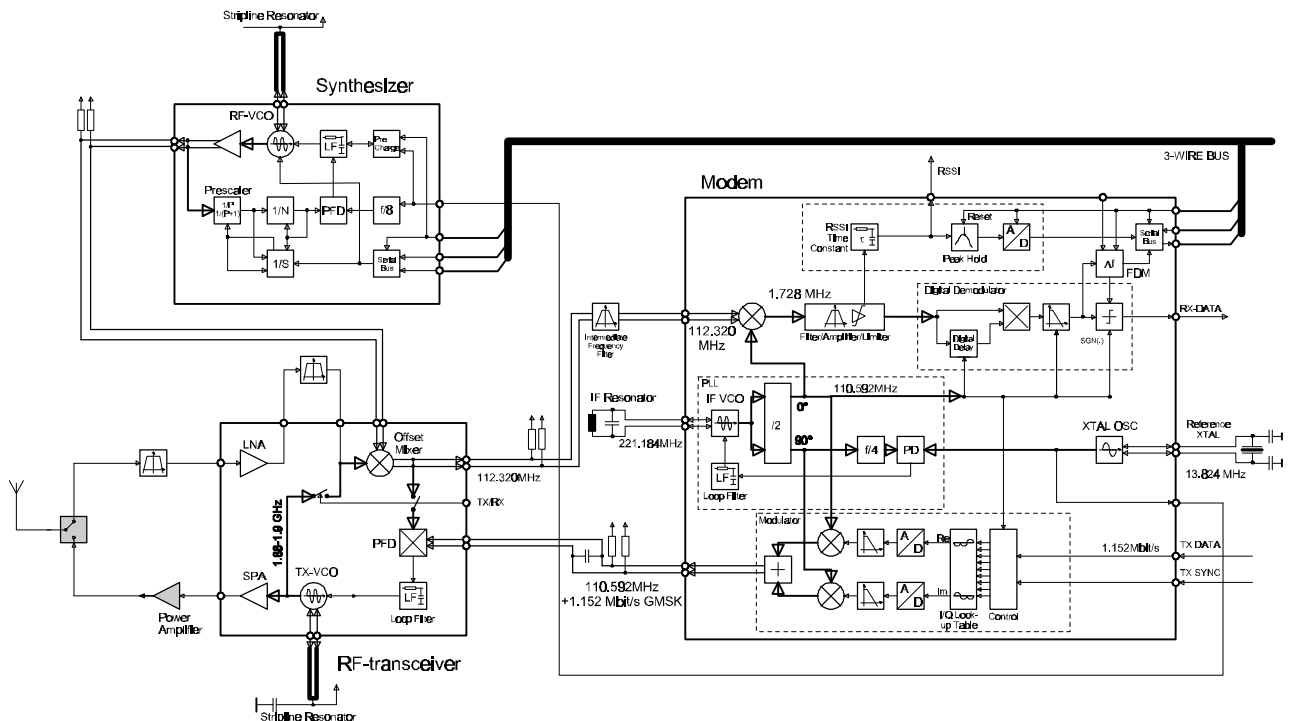
Figure 1. DECT radio part application diagram.
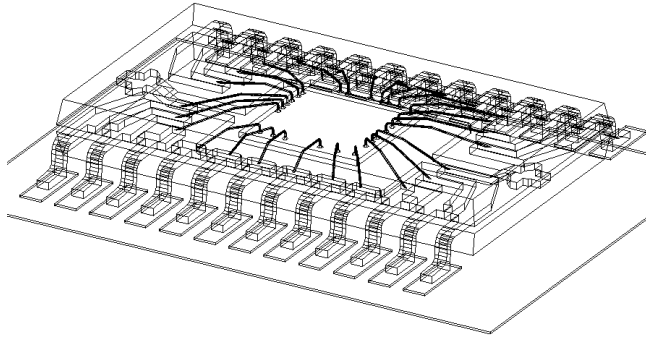
Figure 2. TSSOP package, bondwires and solder-dots used for field simulations.
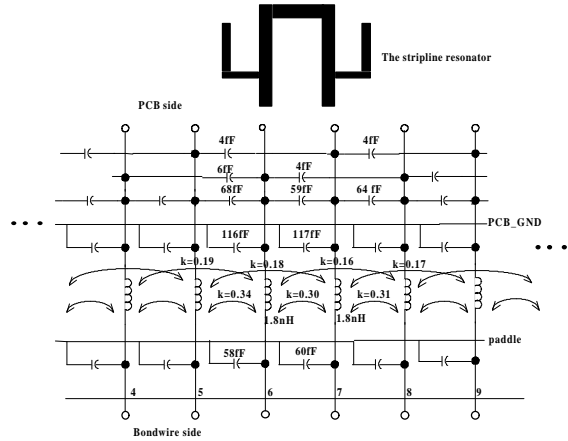
Figure 3. Package and bondwire model around VCO output pins 6 and 7.
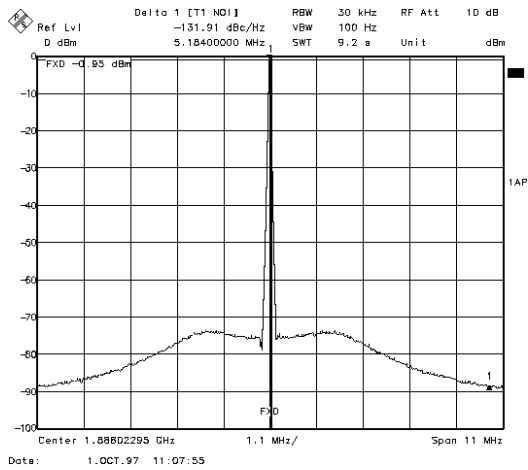
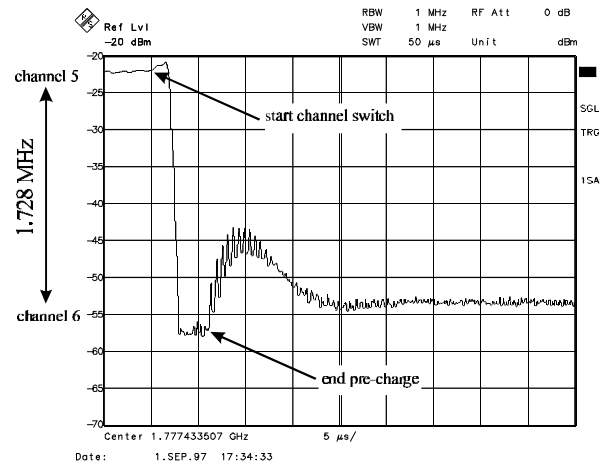Figure 4. RF-Transceiver output spectrum. (no modulation)

Figure 6. Synthesizer response, while switching from channel 5 to 6. (Synthesizer output, Zero Span Mode)
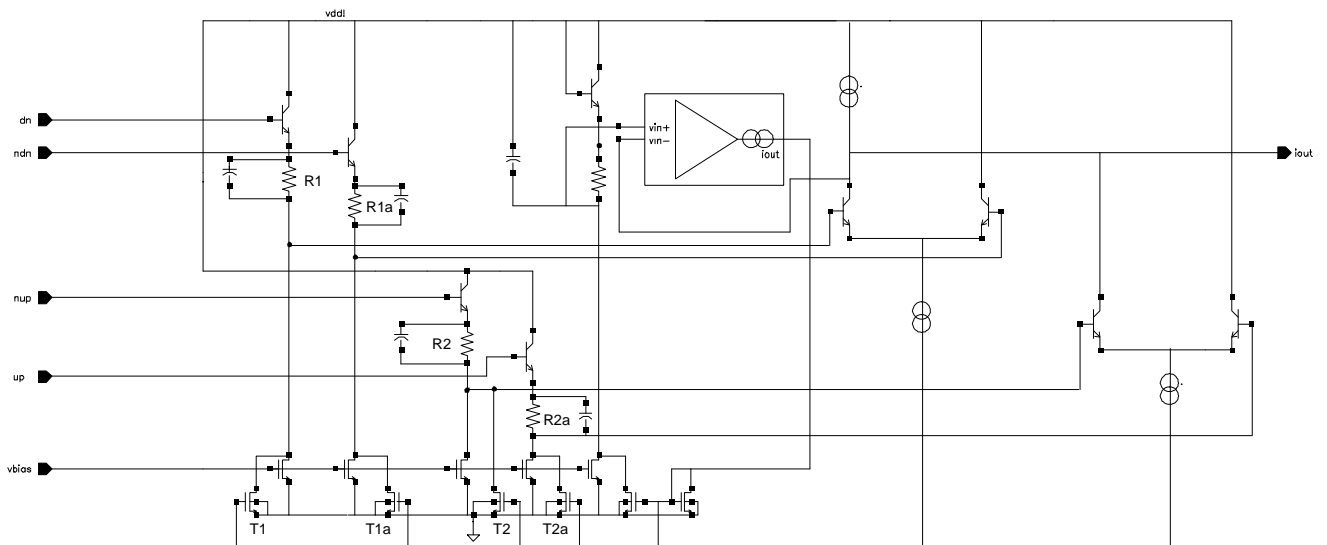

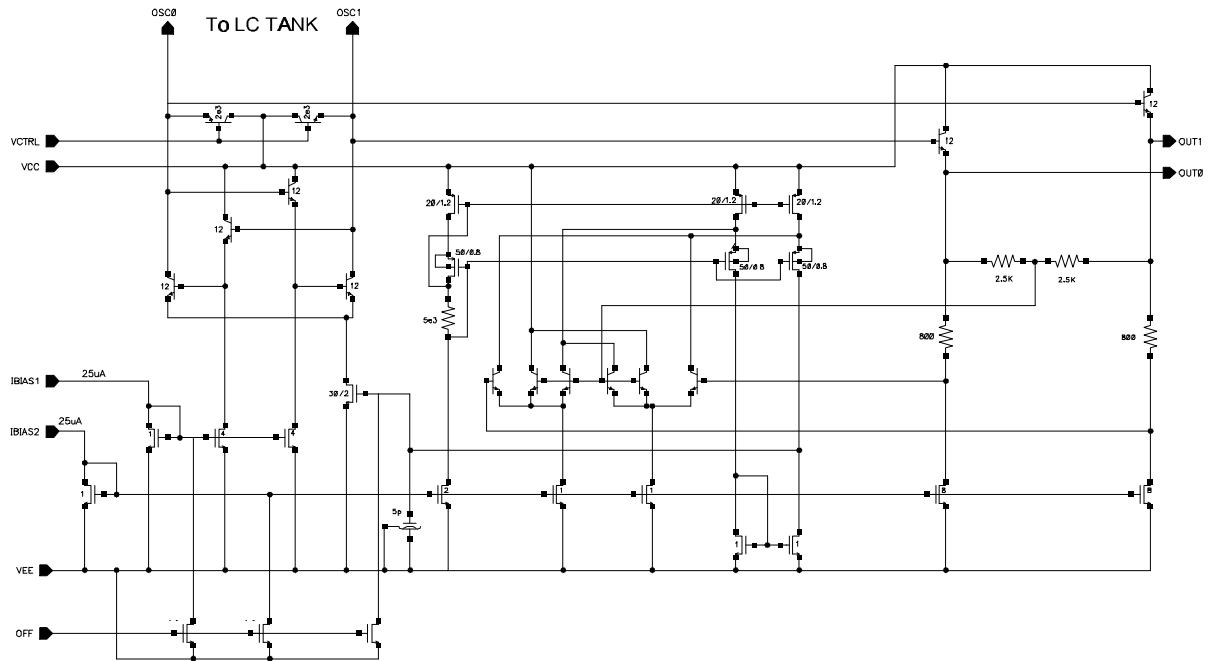Figure 5. 110 MHz Charge Pump with dynamic level shifters.

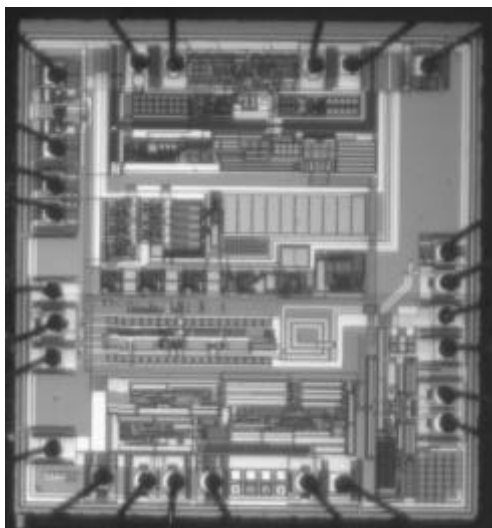Figure 7. VCO with amplitude control.
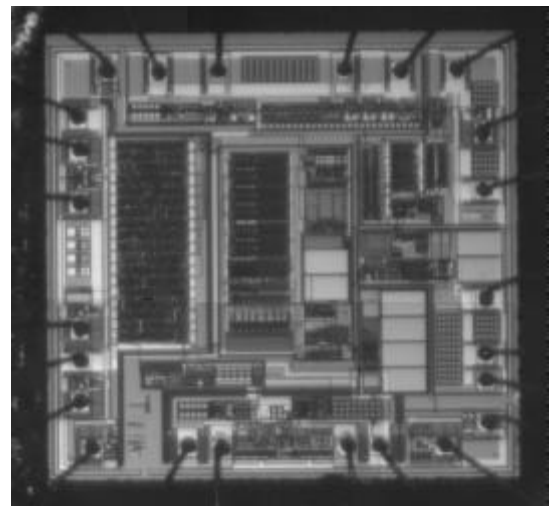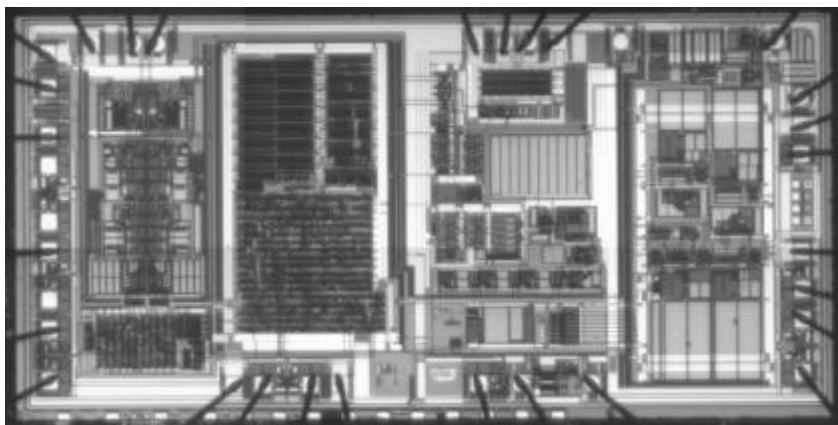

Figure 8. Die photograph RF Transceiver.

Figure 9. Die photograph Synthesizer.

Figure 10. Die photograph Modem.